

Compal Confidential

PEW71/91/51 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibox Peak-M

NV N11P-GV2H and N11P-GE,N12P-GS N12P-GV-OP With Optimus

2010-12-29

REV: 1.0

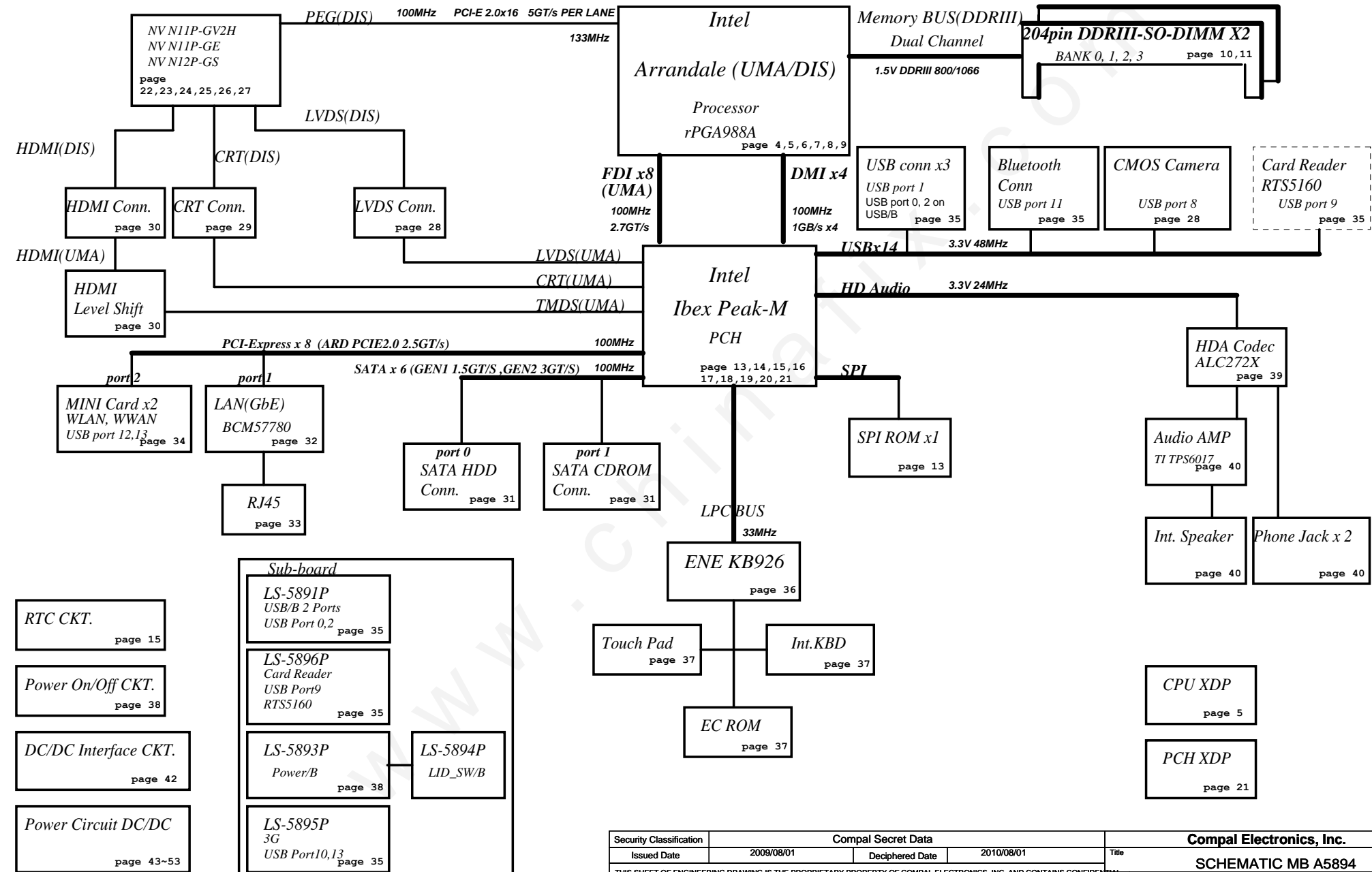
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	SCHEMATIC MB A5894
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				Date	Thursday, January 20, 2011
				Sheet	1 of 56

Compal Confidential

Model Name : PEW71/91/51
File Name : LA5894P

Fan Control
page 41

Clock Generator
IDT: 9LVS3199AKLFT
Realtek: RTM890N-631-VB-GRT
133/120/100/96/14.318MHZ to PCH
page 12



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				Date	Thursday, January 20, 2011
				Sheet	2 of 56

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Config move to page 56

VRAM BOM Config
X7621@: X76198BOL21 ALT. GROUP PARTS 1G SAM
X7622@ X76198BOL22 ALT. GROUP PARTS 1G HYN

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA ONLY	UMA ONLY@
Discrete	DIS@
Discrete Only	DIS ONLY@
VRAM	X76@
Switchable	SG@
UMA ONLY & OPTIMUS	UMOP@
3G	3G@
Blue Tooth	BT@
OPTIMUS	OPT@
NonSG SKU	NonSG@
NEW71	71@
NEW91	91@
N11P-GV2H	GV2H@
N11P-GE1	GE1@
N11P-GV2H-A2	GV2HA2@
N11P-GV2H-A3	GV2HA3@
Non OPT SKU	NonOPT@
SG or OPT	SGOPT@
N11P-GE	GE@
N12P-GS	GS@

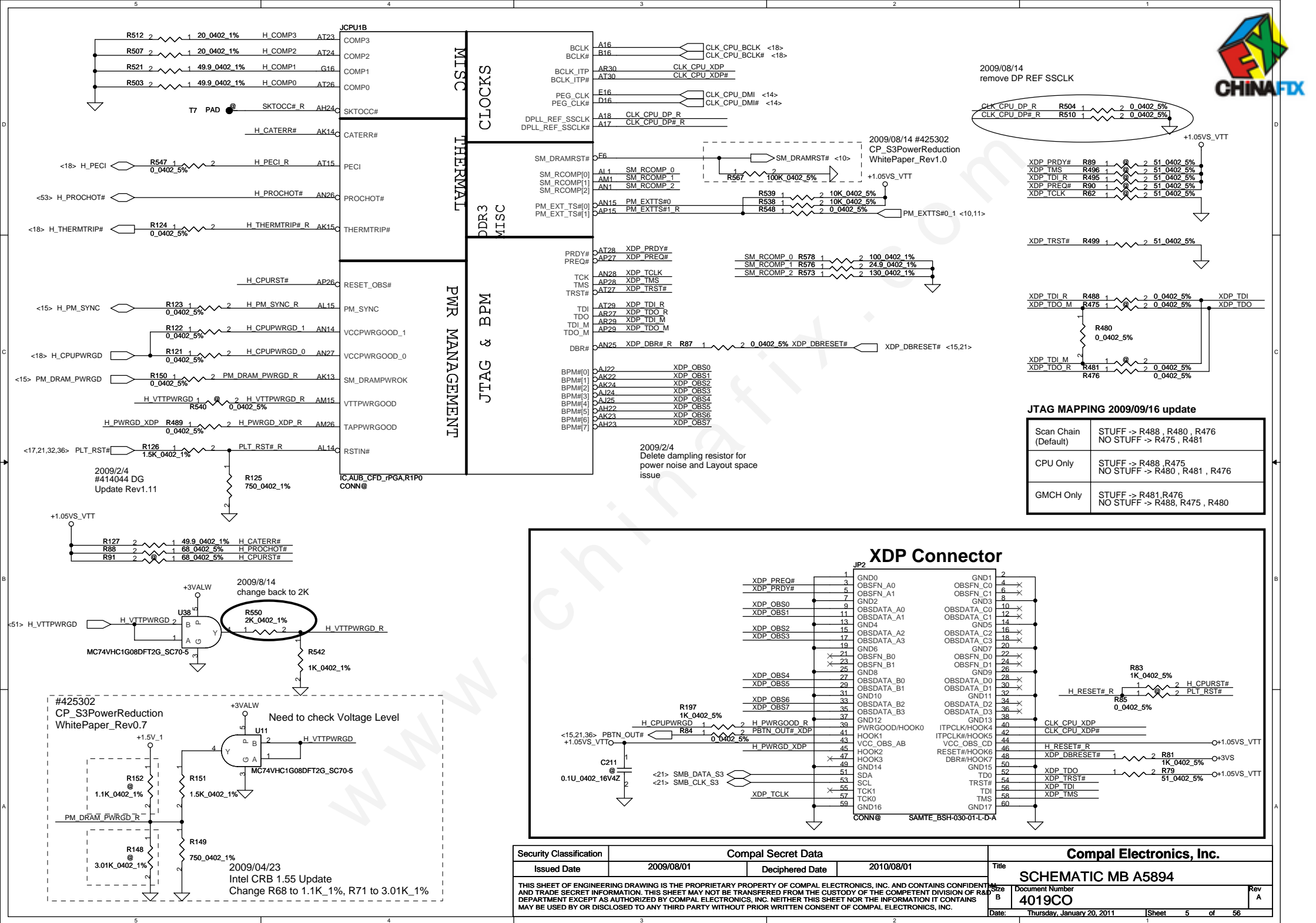
VRAM P/N :
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Card Reader
	UHCI5	10	SIM Card
		11	Blue Tooth
	UHCI6	12	Mini Card(WLAN)
		13	Mini Card(GPS)

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				Date:	Thursday, January 20, 2011
				Sheet	3 of 56





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<10> DDR_A_DM[0..7]
<10> DDR_A_DQS[0..7]
<10> DDR_A_MA[0..15]

JCPU1C

DDR_A_D0 A10
DDR_A_D1 C10
DDR_A_D2 C7
DDR_A_D3 A7
DDR_A_D4 B10
DDR_A_D5 D10
DDR_A_D6 E10
DDR_A_D7 A8
DDR_A_D8 D8
DDR_A_D9 F10
DDR_A_D10 E6
DDR_A_D11 E7
DDR_A_D12 E9
DDR_A_D13 B7
DDR_A_D14 E7
DDR_A_D15 C6
DDR_A_D16 H10
DDR_A_D17 G8
DDR_A_D18 K7
DDR_A_D19 J8
DDR_A_D20 G7
DDR_A_D21 G10
DDR_A_D22 J7
DDR_A_D23 J10
DDR_A_D24 L7
DDR_A_D25 M6
DDR_A_D26 M8
DDR_A_D27 L9
DDR_A_D28 L6
DDR_A_D29 K8
DDR_A_D30 N8
DDR_A_D31 P9
DDR_A_D32 AH5
DDR_A_D33 AF5
DDR_A_D34 AK6
DDR_A_D35 AK7
DDR_A_D36 AE6
DDR_A_D37 AG5
DDR_A_D38 AJ7
DDR_A_D39 AJ6
DDR_A_D40 AJ10
DDR_A_D41 AJ9
DDR_A_D42 AL10
DDR_A_D43 AK12
DDR_A_D44 AK8
DDR_A_D45 AL7
DDR_A_D46 AK11
DDR_A_D47 AL8
DDR_A_D48 AN8
DDR_A_D49 AN10
DDR_A_D50 AR11
DDR_A_D51 AL11
DDR_A_D52 AM9
DDR_A_D53 AN9
DDR_A_D54 AT11
DDR_A_D55 AP12
DDR_A_D56 AM12
DDR_A_D57 AN12
DDR_A_D58 AM13
DDR_A_D59 AT14
DDR_A_D60 AT12
DDR_A_D61 AL13
DDR_A_D62 AR14
DDR_A_D63 AP14

IC:AUB_CFD_rPGA,R1P0
CONN@

DDR SYSTEM MEMORY A

SA_CK[0] AA6
SA_CK[1] AA7
SA_CKE[0] P7
SA_CK[1] Y6
SA_CK[1] Y6
SA_CKE[1] P6
SA_CS[0] AE2
SA_CS[1] AE8
SA_ODT[0] AD8
SA_ODT[1] AF9
SA_DM[0] B9
SA_DM[1] D7
SA_DM[2] H7
SA_DM[3] M7
SA_DM[4] AG6
SA_DM[5] AM7
SA_DM[6] AN10
SA_DM[7] AN13
SA_DQS[0] C9
SA_DQS[1] E8
SA_DQS[2] J8
SA_DQS[3] AG9
SA_DQS[4] AH7
SA_DQS[5] AK9
SA_DQS[6] AP11
SA_DQS[7] AT13
SA_DQS[0] C8
SA_DQS[1] E9
SA_DQS[2] H9
SA_DQS[3] M9
SA_DQS[4] AH8
SA_DQS[5] AK10
SA_DQS[6] AN11
SA_DQS[7] AR13
SA_MA[0] Y3
SA_MA[1] W1
SA_MA[2] AA8
SA_MA[3] AA3
SA_MA[4] V1
SA_MA[5] AA9
SA_MA[6] V8
SA_MA[7] T1
SA_MA[8] Y9
SA_MA[9] U6
SA_MA[10] AD4
SA_MA[11] T2
SA_MA[12] U3
SA_MA[13] AG8
SA_MA[14] T3
SA_MA[15] V9
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DDR_A_MA9
DDR_A_MA10
DDR_A_MA11
DDR_A_MA12
DDR_A_MA13
DDR_A_MA14
DDR_A_MA15

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SA_BS[2]
SA_CAS#
SA_RAS#
SA_WE#

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DDR_A_RAS# AB3C
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<11> DDR_B_DQS[0..7]
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JCPU1D

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DDR_B_D2 C3
DDR_B_D3 B3
DDR_B_D4 E4
DDR_B_D5 A6
DDR_B_D6 C4
DDR_B_D7 D1
DDR_B_D8 D1
DDR_B_D9 D2
DDR_B_D10 F2
DDR_B_D11 E1
DDR_B_D12 C2
DDR_B_D13 E5
DDR_B_D14 F3
DDR_B_D15 G4
DDR_B_D16 H6
DDR_B_D17 G2
DDR_B_D18 J6
DDR_B_D19 J3
DDR_B_D20 G1
DDR_B_D21 G5
DDR_B_D22 J2
DDR_B_D23 J1
DDR_B_D24 J5
DDR_B_D25 K2
DDR_B_D26 L3
DDR_B_D27 M1
DDR_B_D28 K5
DDR_B_D29 K4
DDR_B_D30 M4
DDR_B_D31 N5
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DDR_B_D33 AG1
DDR_B_D34 AJ3
DDR_B_D35 AK1
DDR_B_D36 AG4
DDR_B_D37 AG3
DDR_B_D38 AJ4
DDR_B_D39 AH4
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DDR_B_D41 AK3
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DDR_B_D43 AN2
DDR_B_D44 AK5
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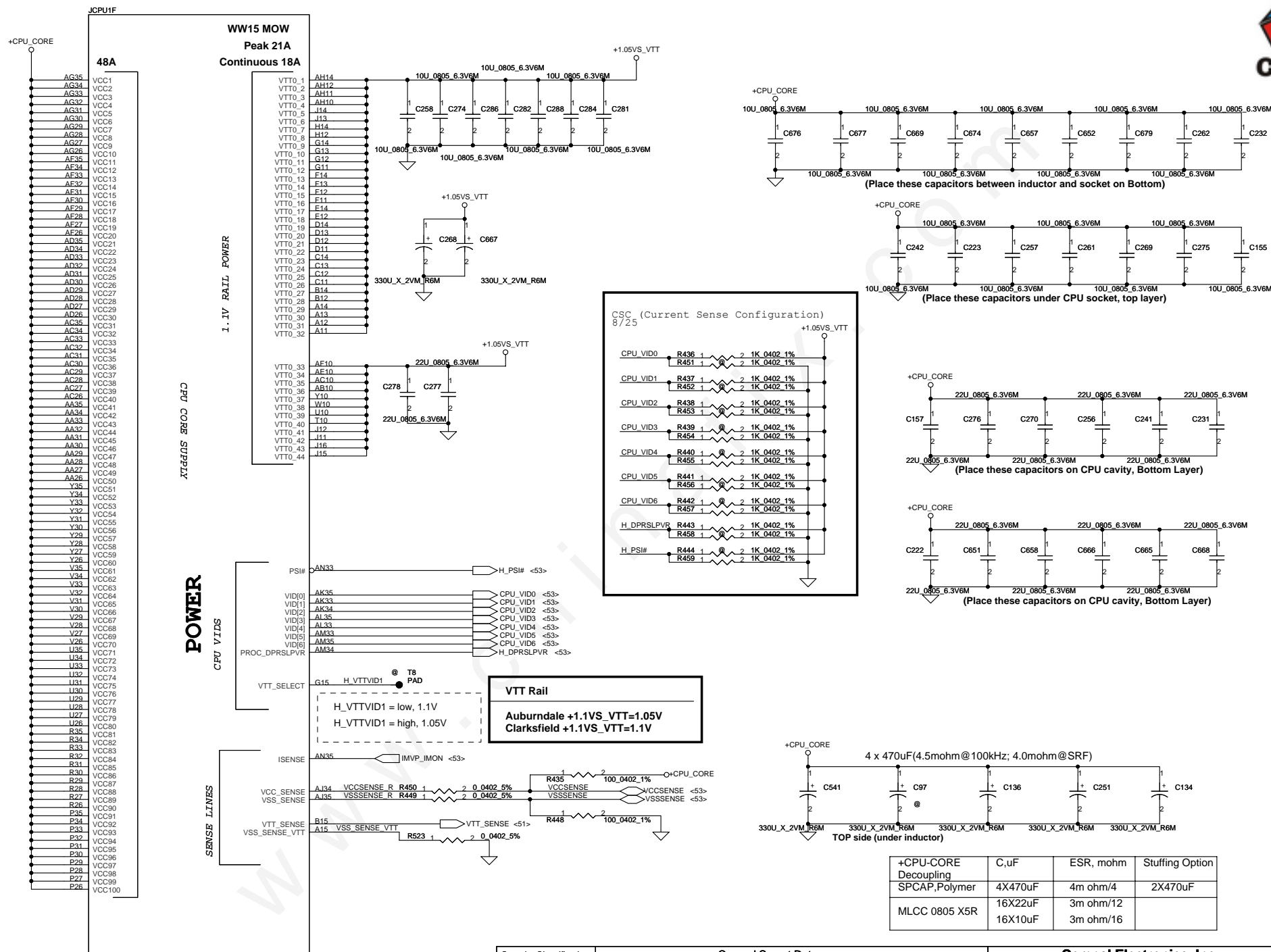
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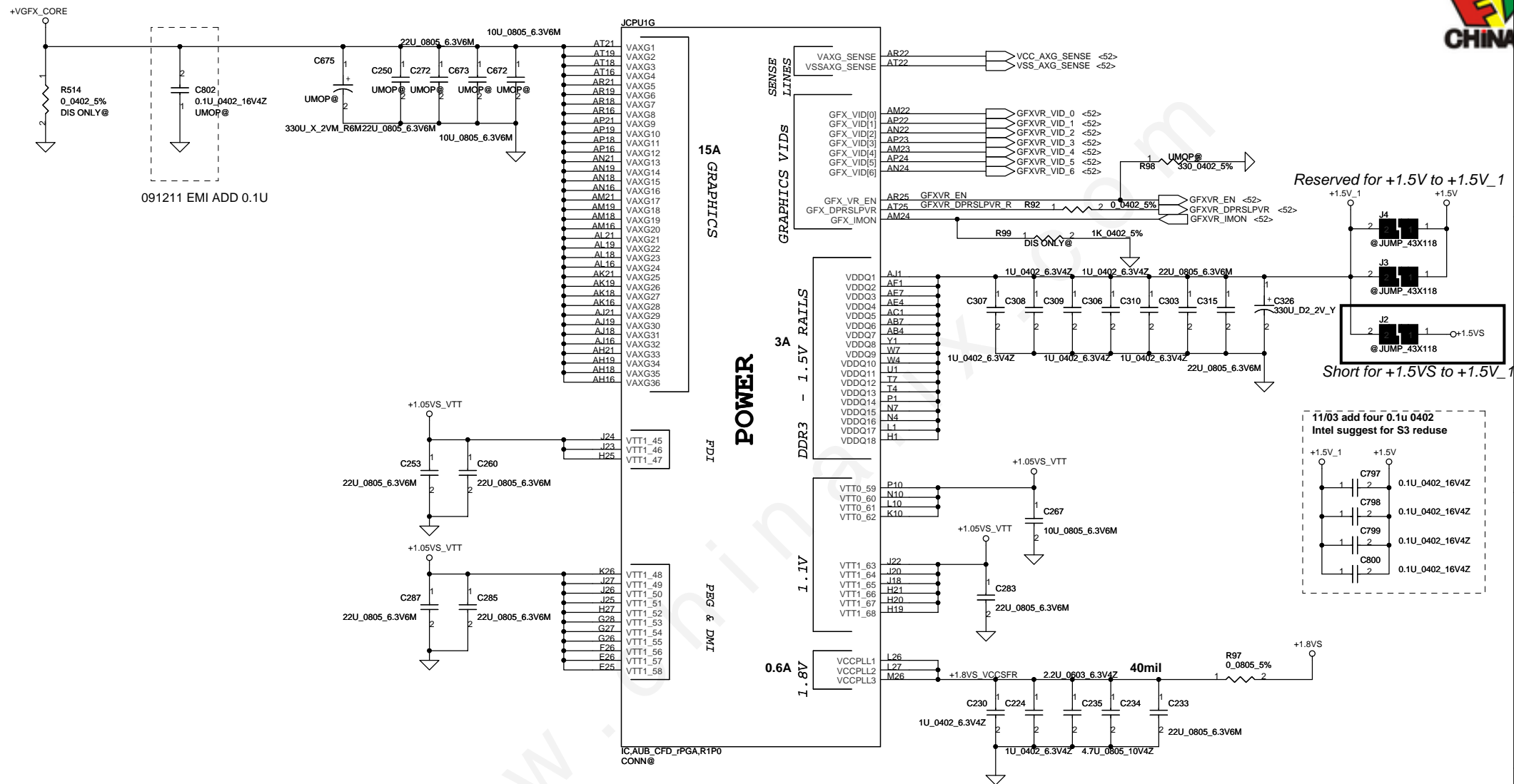
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SB_CS[1] AD6
SB_ODT[0] AC7
SB_ODT[1] AD1
SB_DM[0] D4
SB_DM[1] E1
SB_DM[2] H3
SB_DM[3] K1
SB_DM[4] AH1
SB_DM[5] AL2
SB_DM[6] AR4
SB_DM[7] AT8
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SB_DQS[3] D4
SB_DQS[4] AH2
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SB_MA[8] R4
SB_MA[9] R5
SB_MA[10] AR5
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SB_MA[12] R3
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DDR_B_DM4
DDR_B_DM5
DDR_B_DM6
DDR_B_DM7
DDR_B_DQS#0
DDR_B_DQS#1
DDR_B_DQS#2
DDR_B_DQS#3
DDR_B_DQS#4
DDR_B_DQS#5
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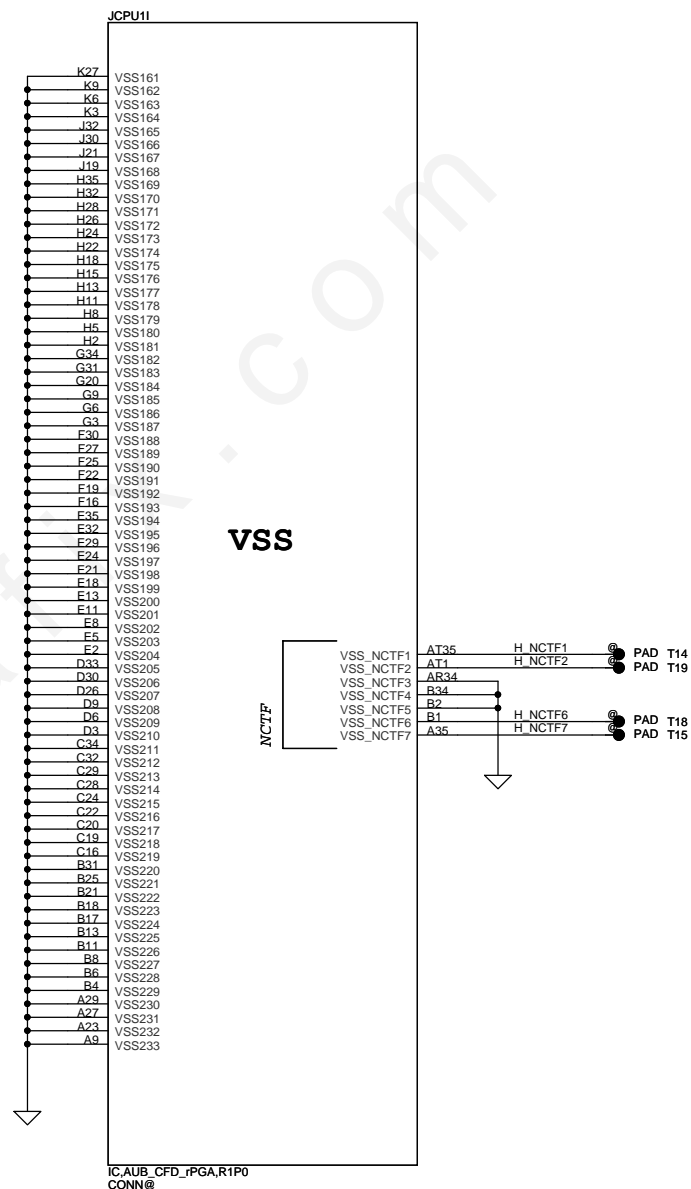


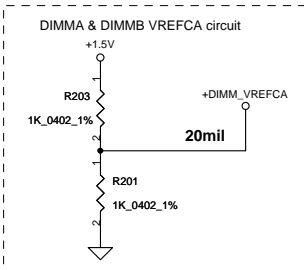
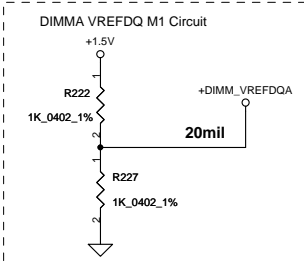
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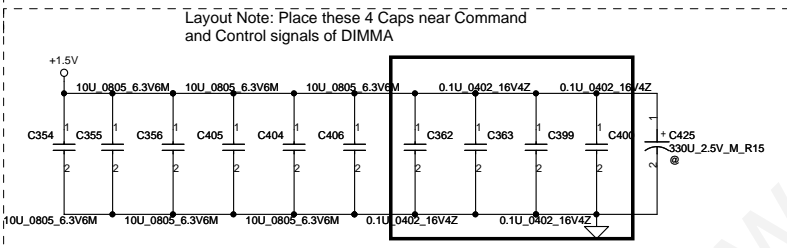


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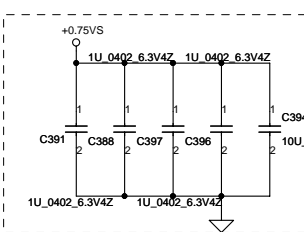




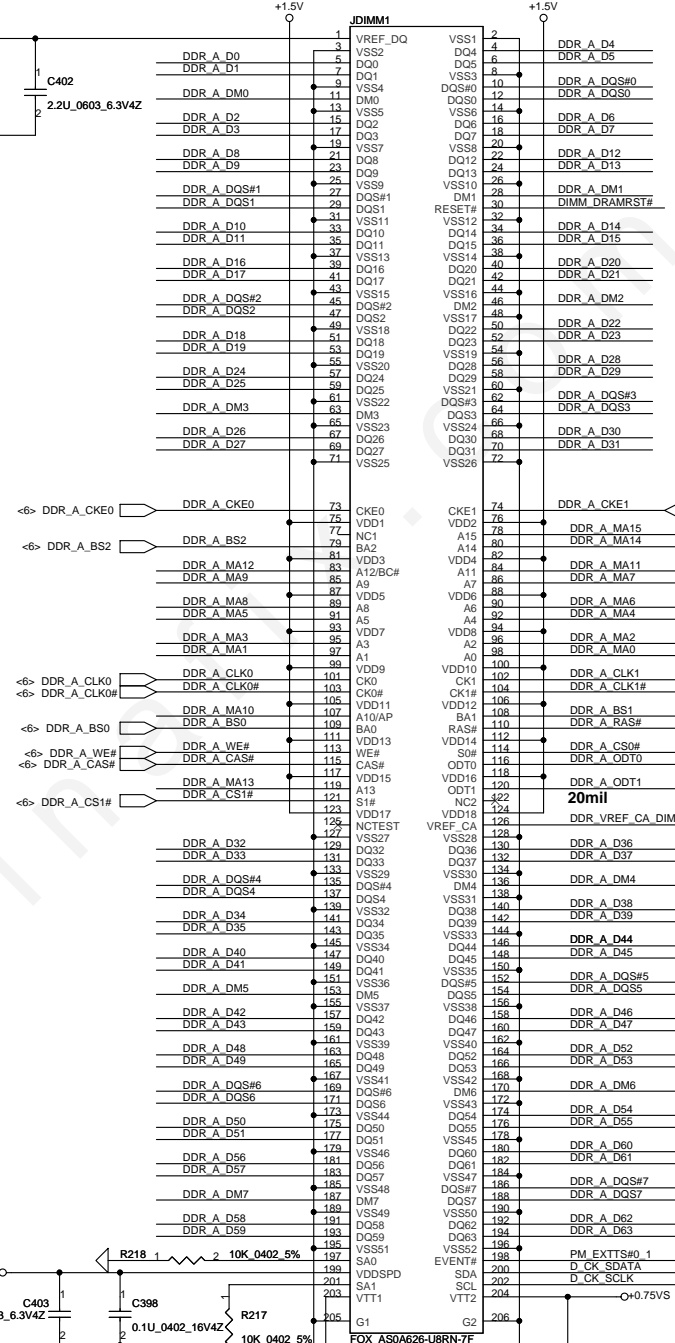
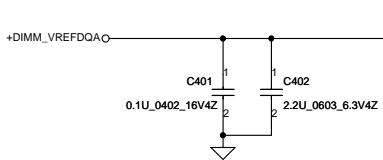
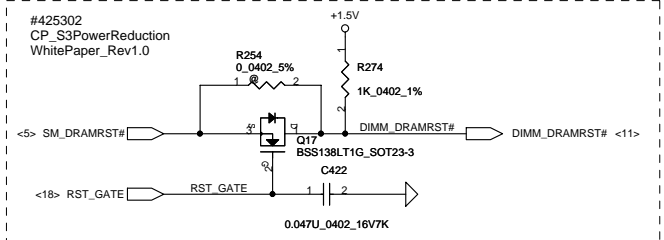
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203 & JDIMM1.204



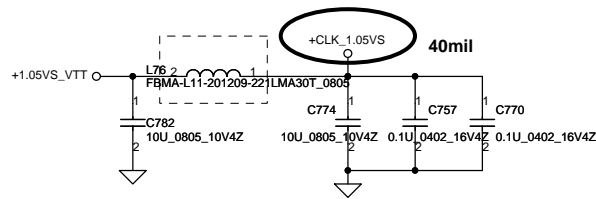
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<6> DDR_A_DQS[0..7]
<6> DDR_A_MA[0..15]



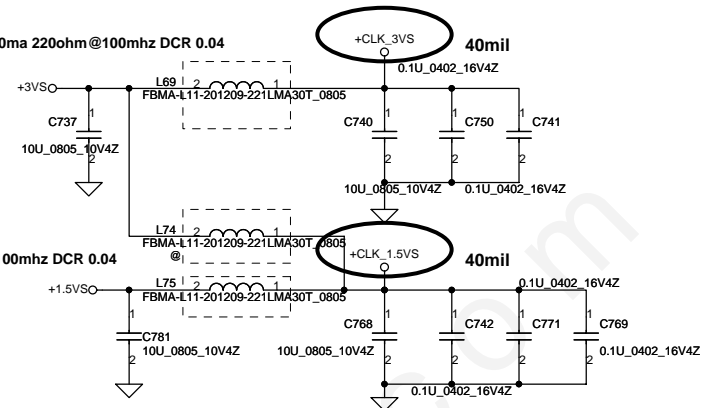
**DDR3 SO-DIMM A
H=8mm**

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								SCHEMATIC MB A5894	
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						4019CO			
						Date: Thursday, January 20, 2011		Sheet 10 of 56	

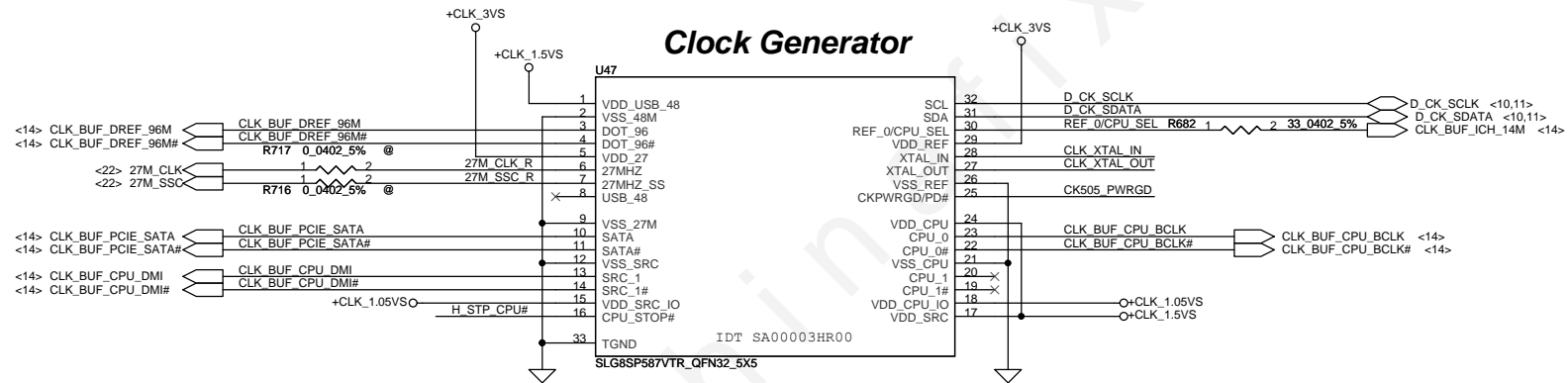
SM010014520 3000ma 220ohm@100mhz DCR 0.04



SM010014520 3000ma 220ohm@100mhz DCR 0.04



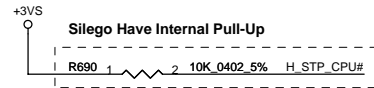
SM010014520 3000ma 220ohm@100mhz DCR 0.04



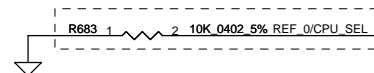
Clock Generator

IDT: 9LRS3199AKLFT, SA00003P00
SILEGO: SLG8SP587V(WF), SA00002XY10
Low Power:
IDT: 9LVS3199AKLFT, SA00003HR00
Realtek: RTM890N-631-VB-GRT, SA00003HQ10

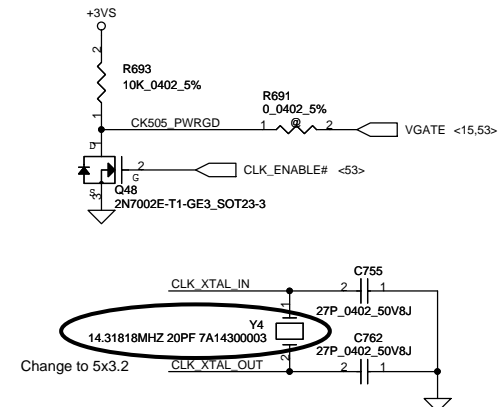
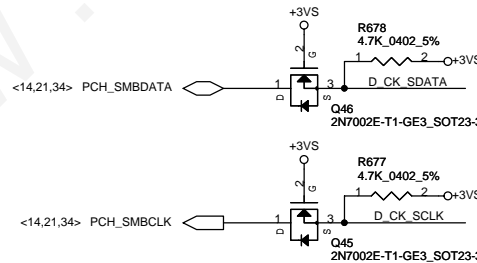
IDT 9LVS3199AKLFT NC



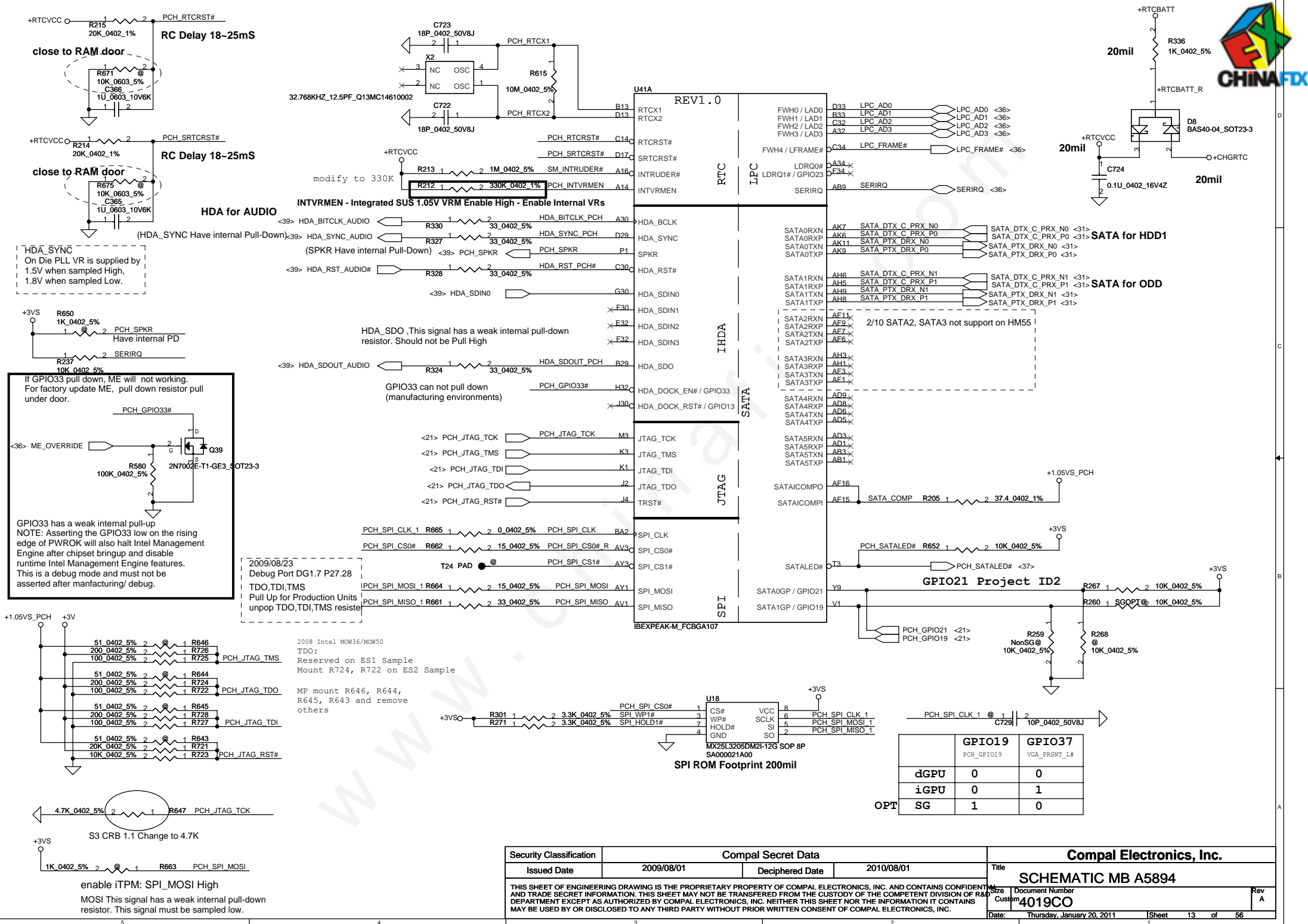
IDT Have Internal Pull-Down
FOR Realtek



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



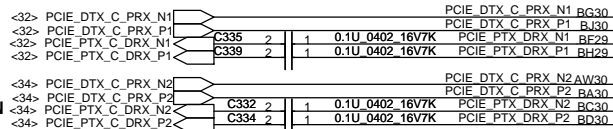
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				Date	Thursday, January 20, 2011
				Sheet	12 of 56



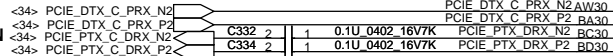


1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

For PCIE LAN



For Wireless LAN

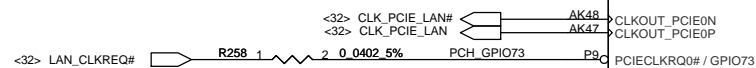


For Mini2

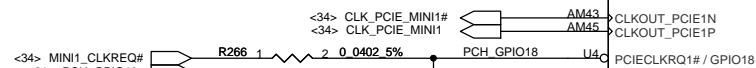
2009/08/25: remove PCIE5

2/10 PCIE7, PCIE8 not support on HM55

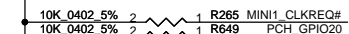
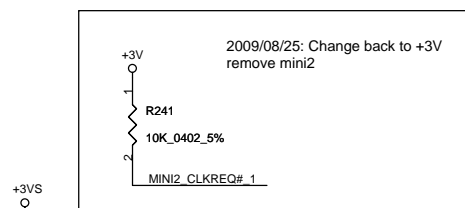
For PCIE LAN



For Wireless LAN



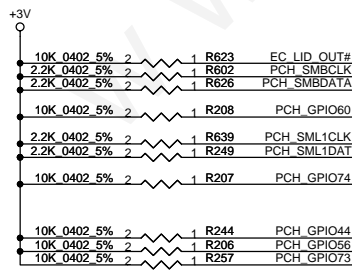
2009/08/25: Change back to +3V
remove mini2



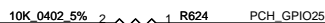
Schematic_Checklist_Rev1.6

GPIO18 Main (core) power well (+V3.3S)
Mixed with PCIECLKRQ1#.
If not used, requires 8.2-k to 10-k pull-up to +Vcc_3.3 (+V3.3S)

GPIO25 Resume (Sus) well (+V3.3A)
Mixed with PCIECLKRQ3#
If not used, requires 8.2-k to 10-k pull-up to +V3.3A rail.

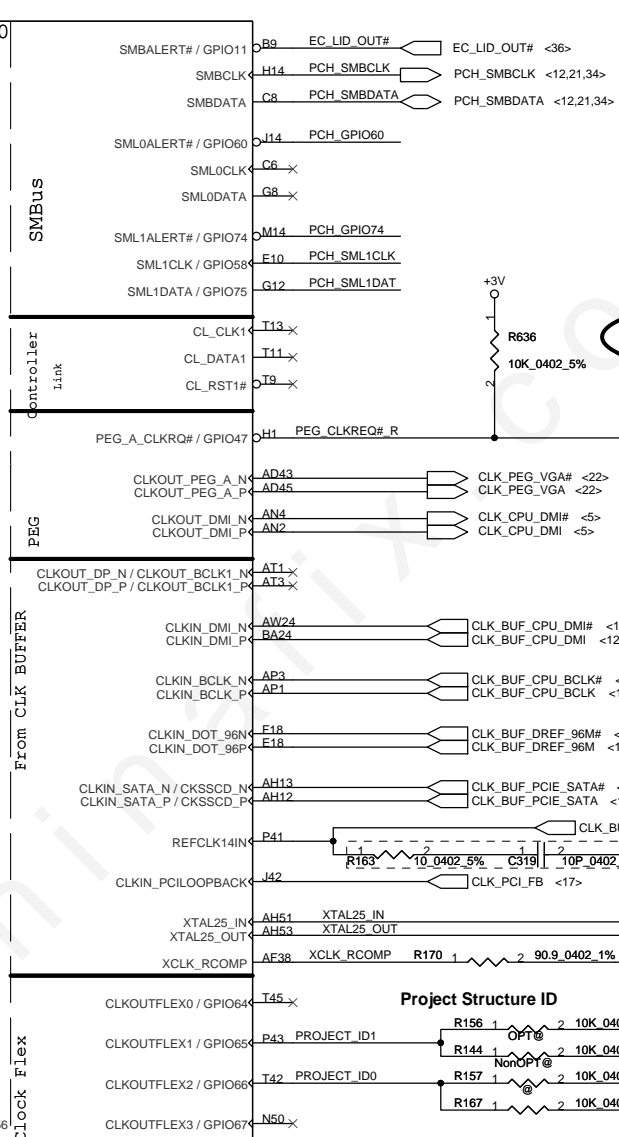


9/1: Change to +3VS
2009/08/13: Change back to +3V

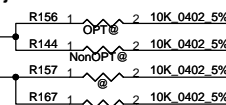


U1B REV1.0

PCI-E



Project Structure ID



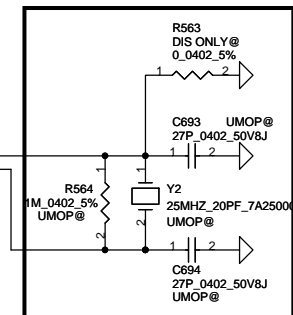
Project Structure

GPIO21 ID2	GPIO65 ID1	GPIO66 ID0	Structure
0	0	0	NEW70
0	0	1	NEW80
0	1	0	NEW90
1	0	0	NEW71/91
1	1	0	NEW71/91

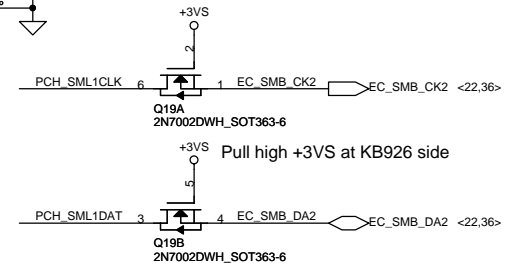
*Discrete

*Optimus

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

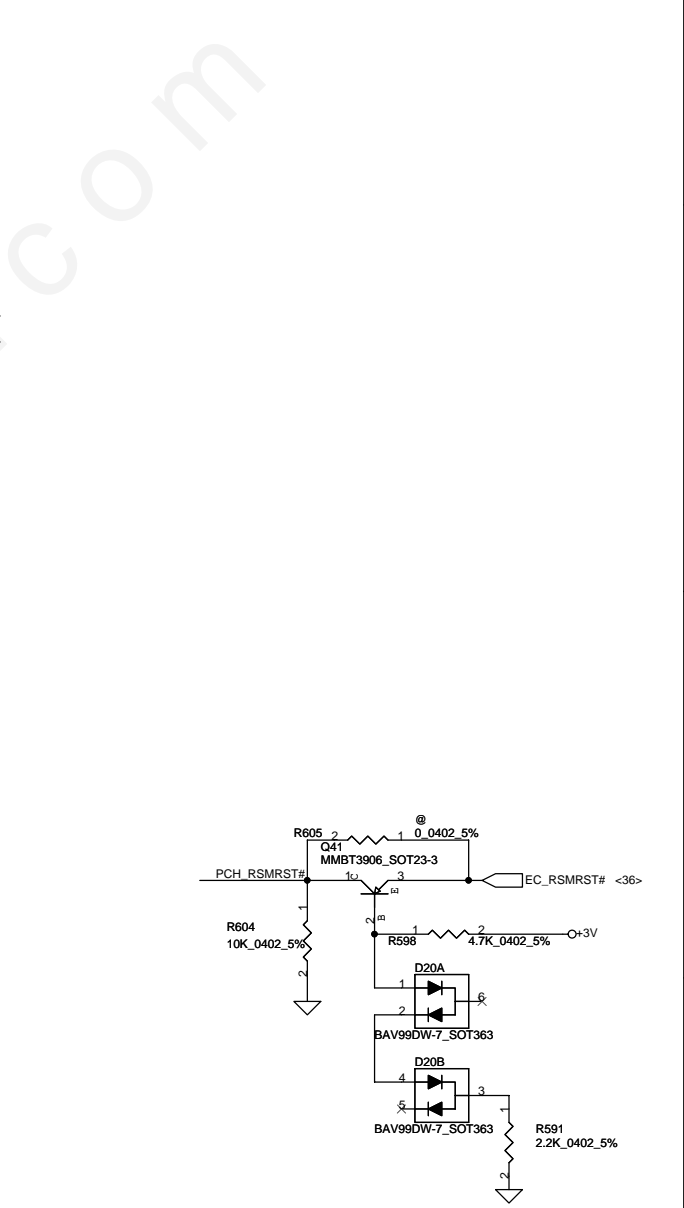
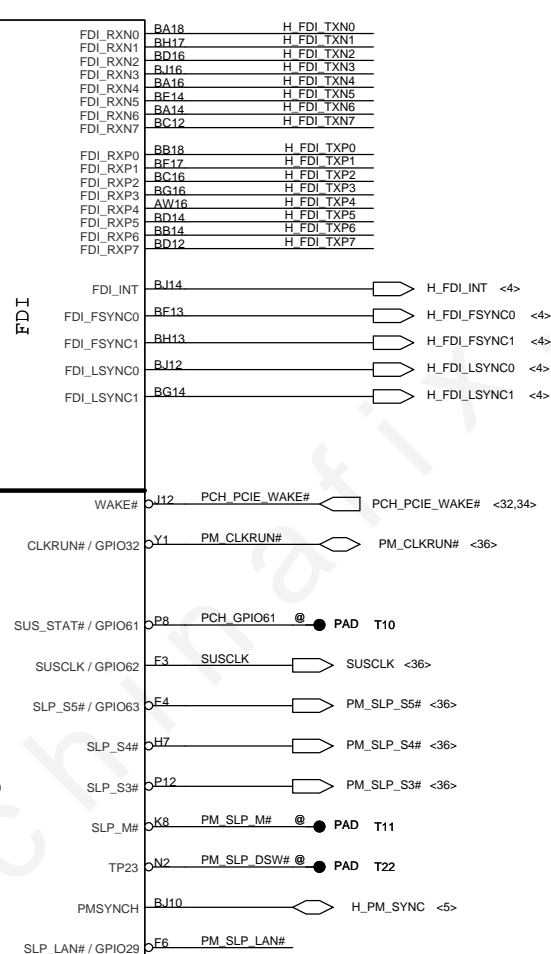
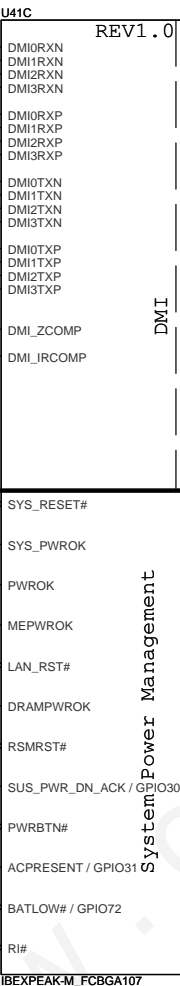
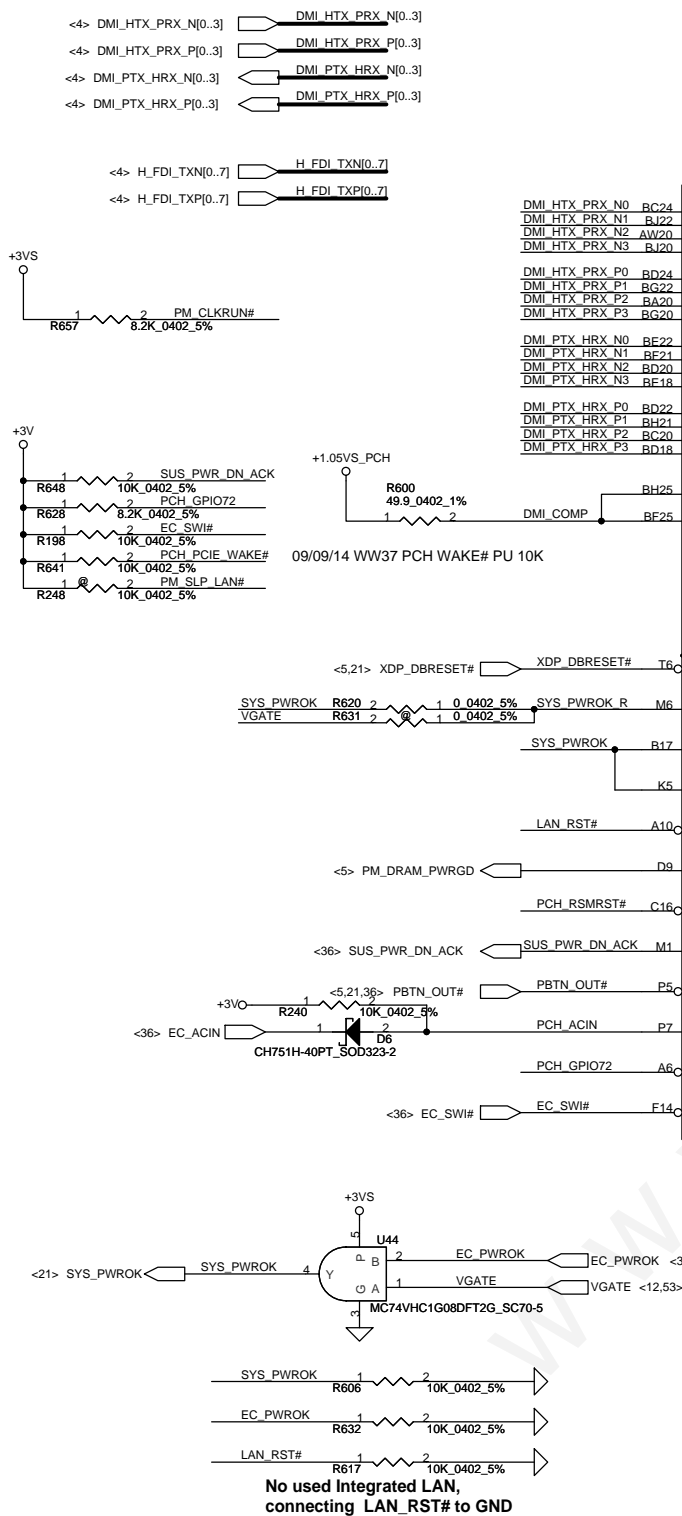


Change to 5x3.2

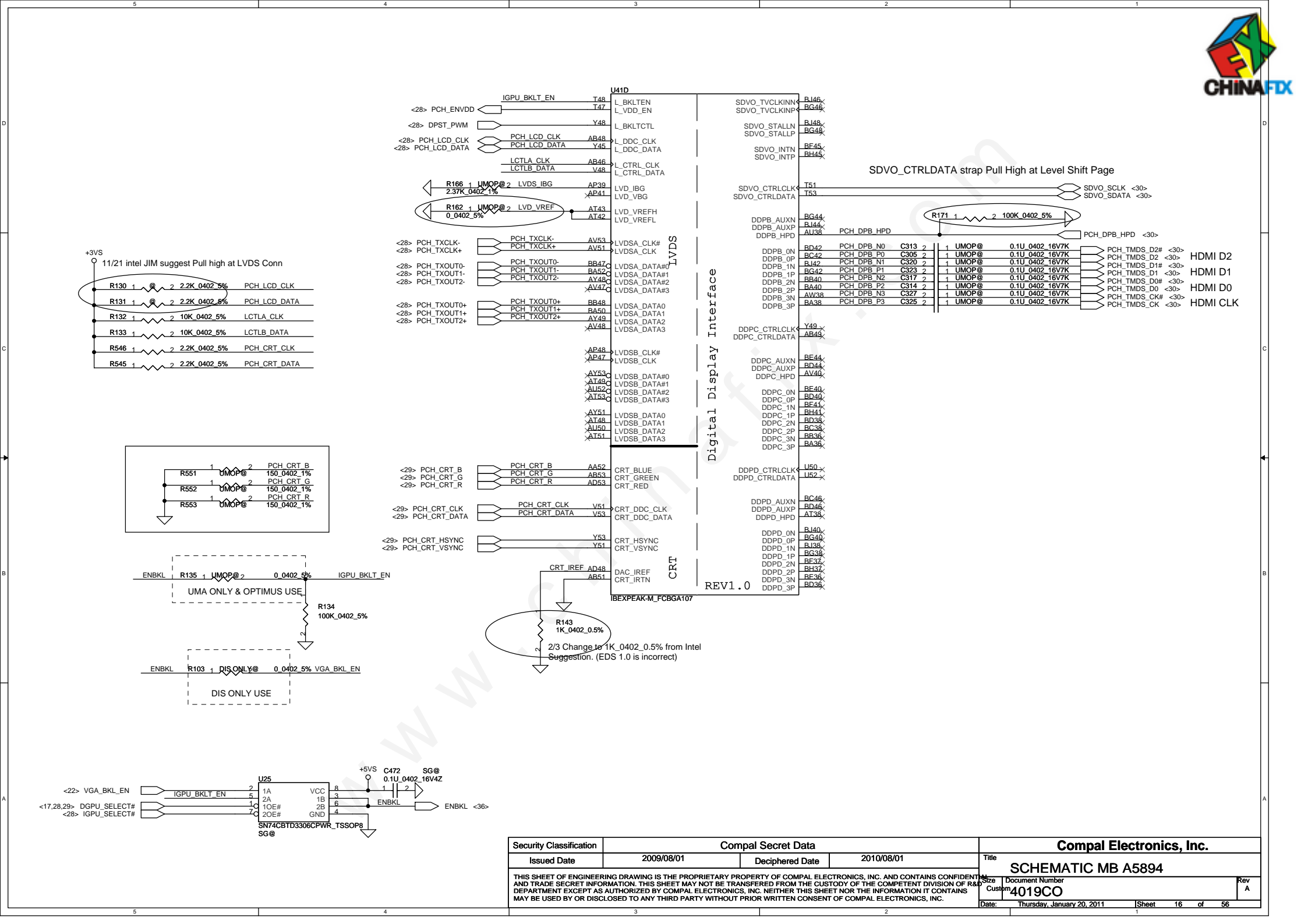
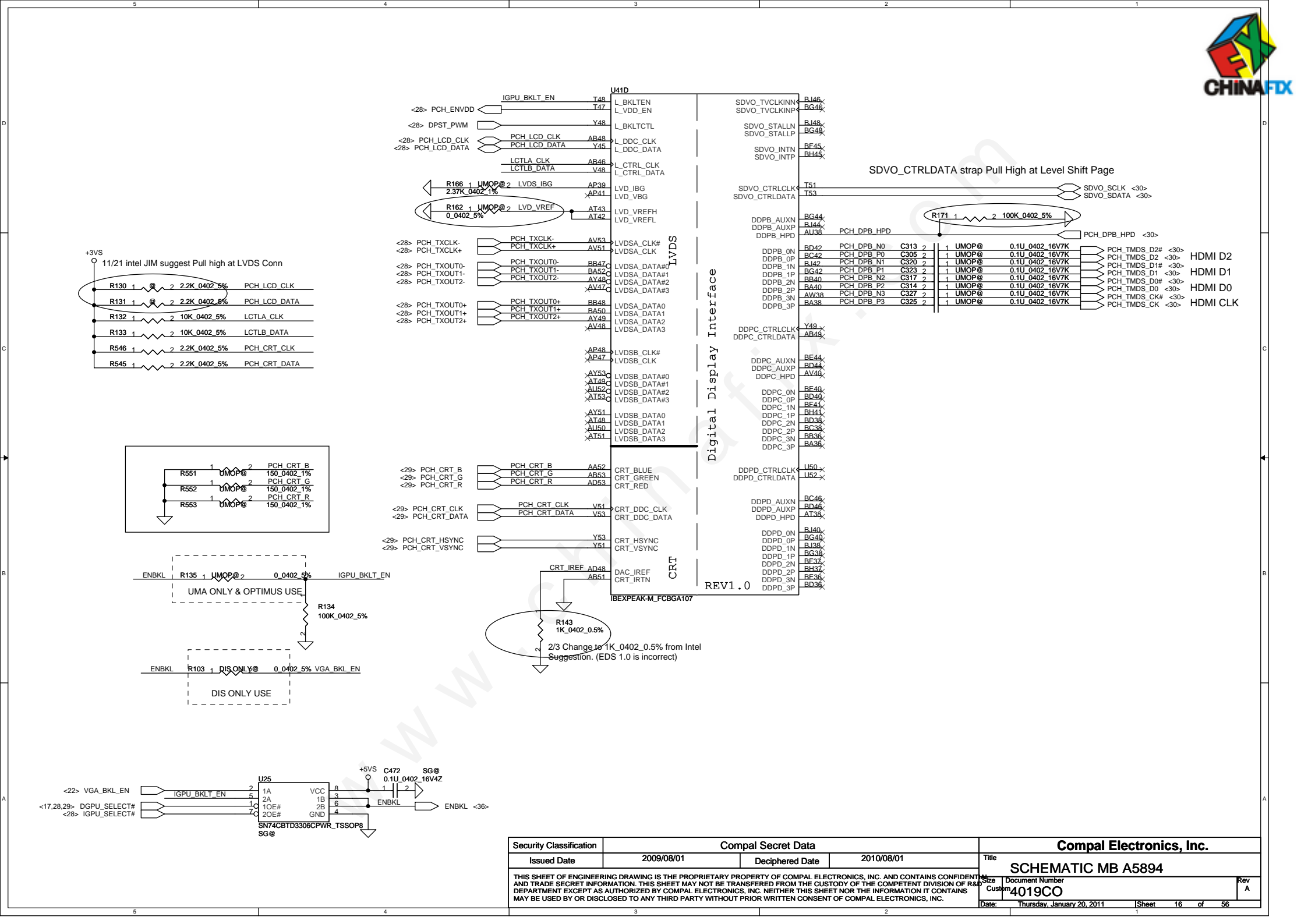


Pull high +3VS at KB926 side

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						Customer		4019CO		A			
						Date:		Thursday, January 20, 2011		Sheet		15 of 56	



LVDS Interface

11/21 intel JIM suggest Pull high at LVDS Conn

R130 1 2.2K 0402 5% PCH_LCD_CLK

R131 1 2.2K 0402 5% PCH_LCD_DATA

R132 1 10K 0402 5% LCTLA_CLK

R133 1 10K 0402 5% LCTLB_DATA

R546 1 2.2K 0402 5% PCH_CRT_CLK

R545 1 2.2K 0402 5% PCH_CRT_DATA

R166 1 UMOP@ 2 2.37K 0402 1% LVDS_IBG

R162 1 UMOP@ 2 0.0402 5% LVDS_VREF

R551 1 UMOP@ 2 150.0402 1% PCH_CRT_B

R552 1 UMOP@ 2 150.0402 1% PCH_CRT_G

R553 1 UMOP@ 2 150.0402 1% PCH_CRT_R

R135 1 UMOP@ 2 0.0402 5% IGPU_BKLT_EN

R134 100K 0402 5%

R103 1 DIS ONLY@ 0.0402 5% VGA_BKLT_EN

R143 1K 0402 0.5%

2/3 Change to 1K_0402_0.5% from Intel Suggestion. (EDS 1.0 is incorrect)

Digital Display Interface

SDVO_TVCLKIN# B146

SDVO_TVCLKINP BG46

SDVO_STALLN B148

SDVO_STALLP BG48

SDVO_INTN BF45

SDVO_INTP BH45

SDVO_CTRLCLK T51

SDVO_CTRLDATA T53

SDVO_SCLK <30>

SDVO_SDATA <30>

DDPB_AUXN BG44

DDPB_AUXP B144

DDPB_HPDP AU38

PCH_DPB_HPDP <30>

DDPB_ON BD42

DDPB_0P BC42

DDPB_1N B142

DDPB_1P BG42

DDPB_2N BD40

DDPB_2P BA40

DDPB_3N DD38

DDPB_3P BA38

DDPC_CTRLCLK Y49

DDPC_CTRLDATA AB49

DDPC_AUXN BE44

DDPC_AUXP BD44

DDPC_HPDP AV40

DDPC_ON BD40

DDPC_0P BE41

DDPC_1N BH41

DDPC_2N BD38

DDPC_2P BC38

DDPC_3N BB38

DDPC_3P BA38

DDPD_CTRLCLK U50

DDPD_CTRLDATA U52

DDPD_AUXN BC46

DDPD_AUXP BD46

DDPD_HPDP AT38

DDPD_ON B140

DDPD_0P BG40

DDPD_1N B138

DDPD_2N BG38

DDPD_2P BE37

DDPD_3N BH37

DDPD_3P BE36

DDPD_3P BD36

CRT Interface

CRT_BLUE AA52

CRT_GREEN AB53

CRT_RED AD53

CRT_DDC_CLK V51

CRT_DDC_DATA V53

CRT_HSYNC Y53

CRT_VSYNC Y51

CRT_IREF AD48

CRT_IRTN AB51

Power Supply

+5VS C472 SG@ 0.1U 0402 16V42

ENBKL

ENBKL <36>

U25

1A VCC

2A 1B

1C 1OE#

2C 2OE#

2OE# GND

SN74CBTD3306CPWR TSSOP8

SG@

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Issued Date 2009/08/01

Deciphered Date 2010/08/01

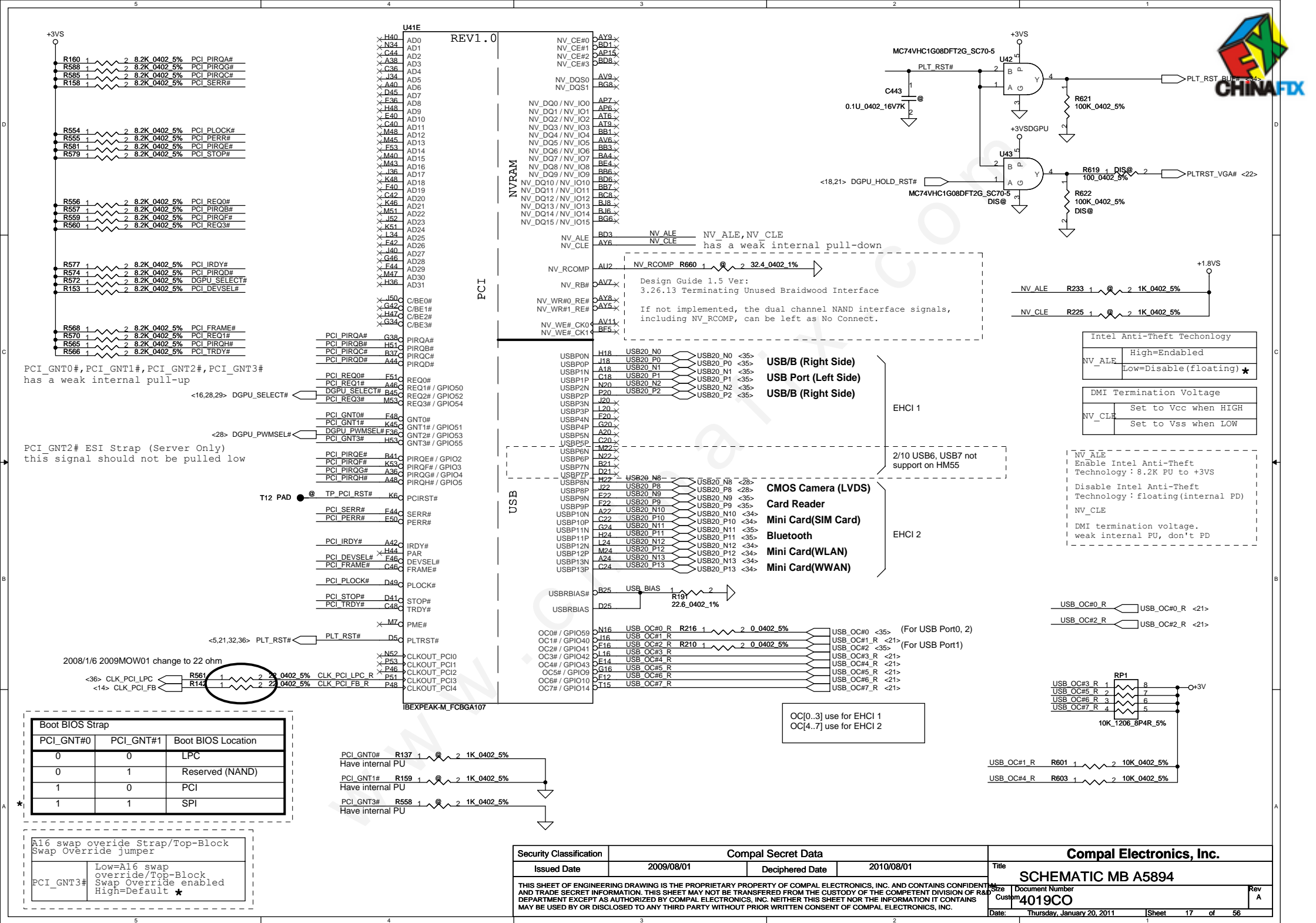
Compal Electronics, Inc.

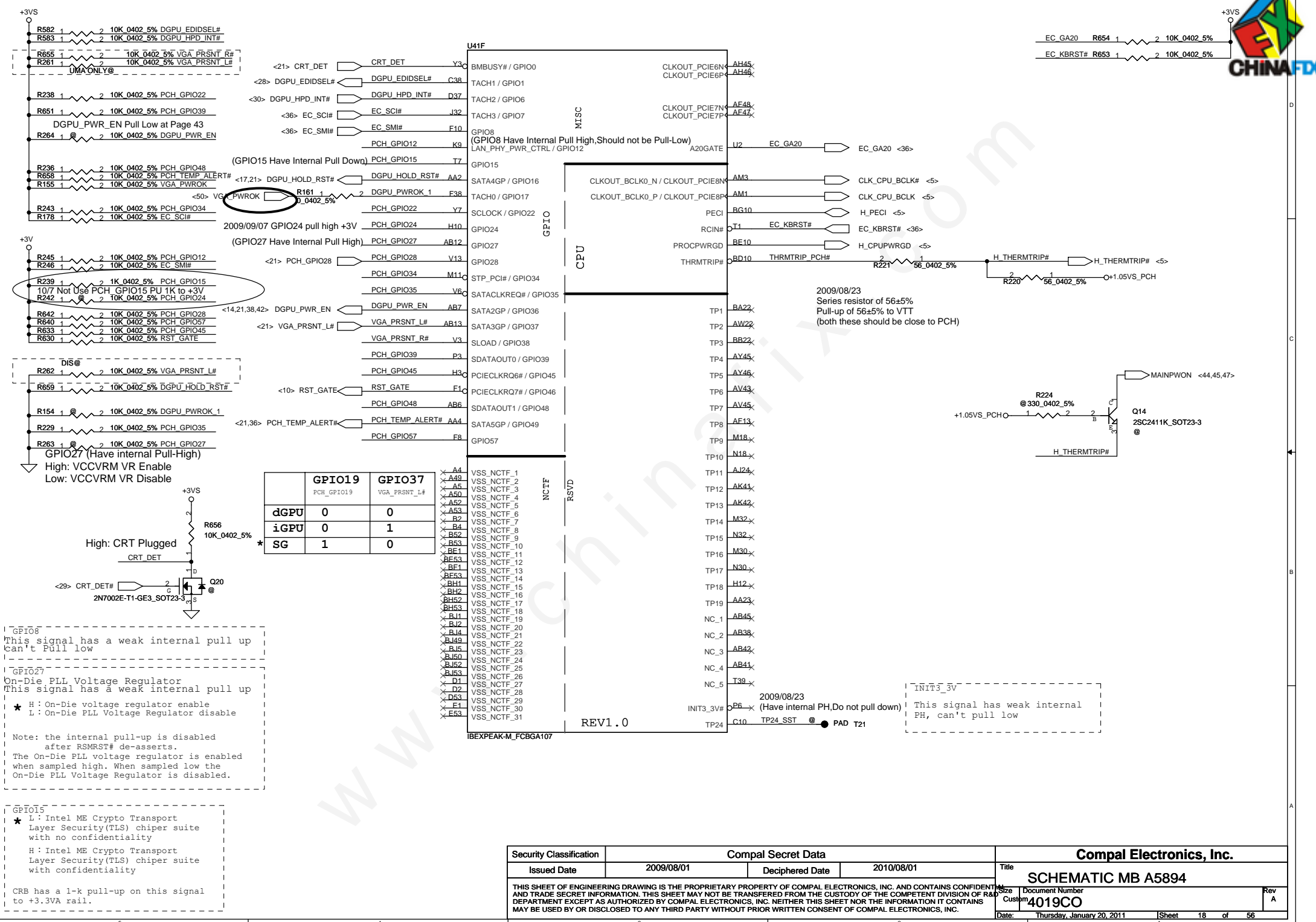
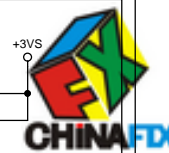
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Document Number 4019CO

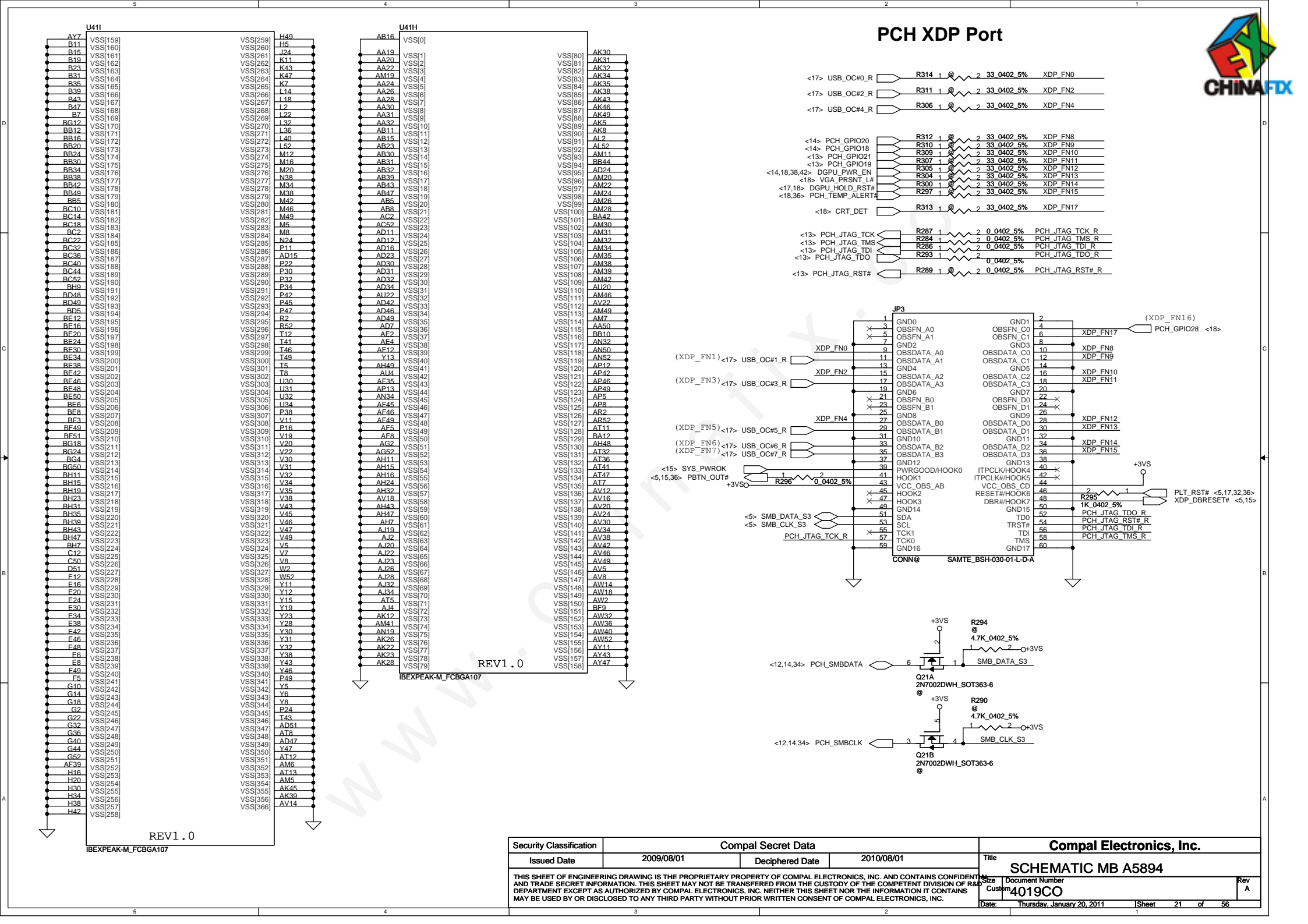
Date Thursday, January 20, 2011

Sheet 16 of 56



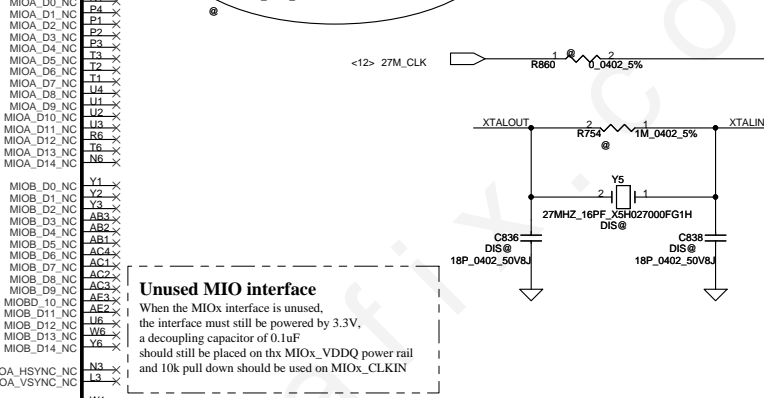
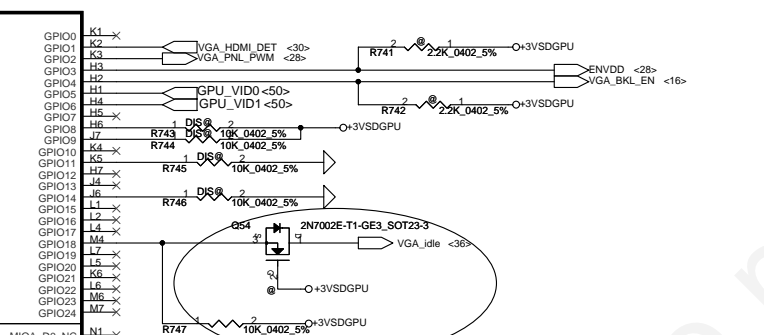




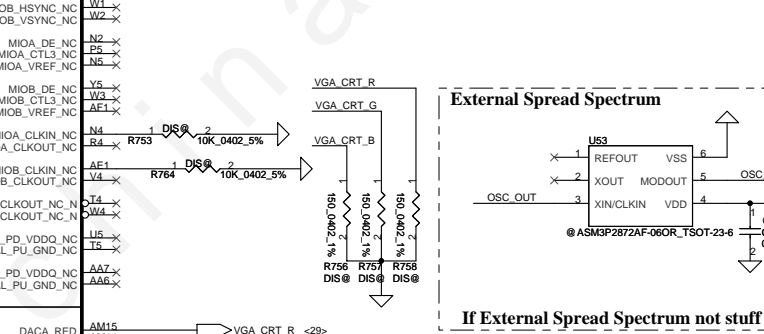




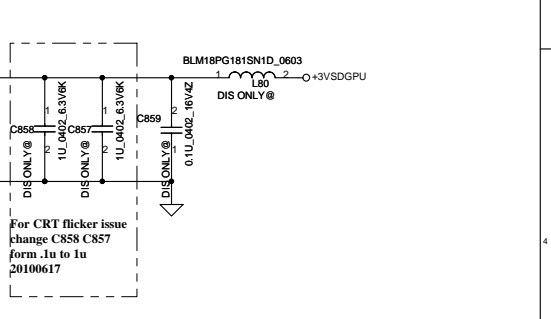
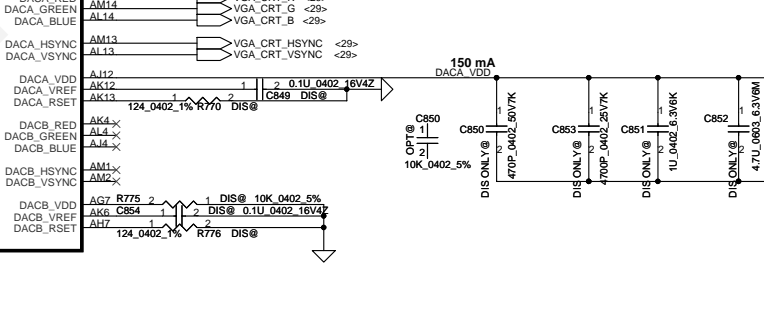
GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_P
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	N/A
GPIO8	IN	L	N/A
GPIO9	OUT	L	N/A
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A



Unused MIO interface
When the MIO interface is unused, the interface must still be powered by 3.3V, a decoupling capacitor of 0.1uF should still be placed on the MIOx_VDD0 power rail and 10k pull down should be used on MIOx_CLKIN



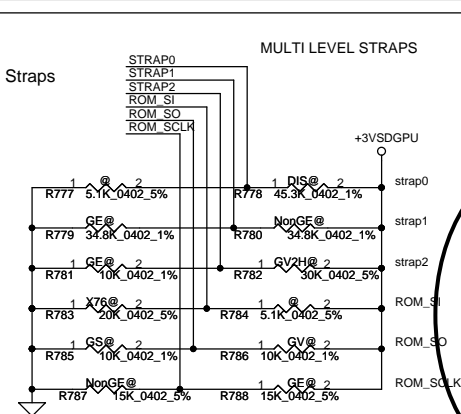
If External Spread Spectrum not stuff then stuff resistor



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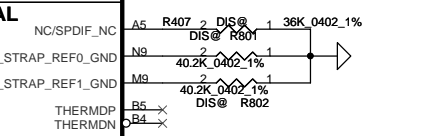
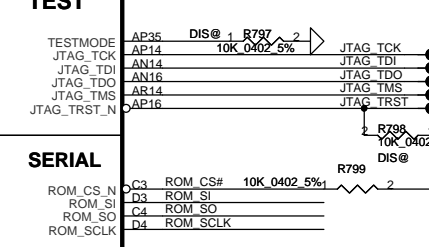
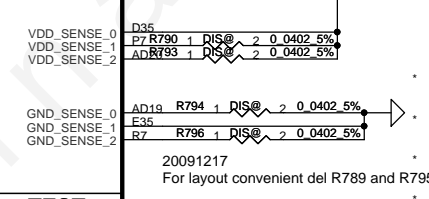
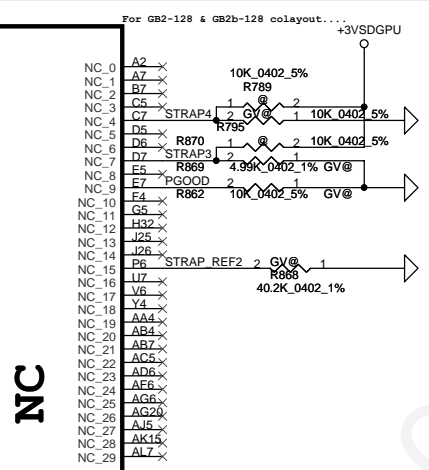
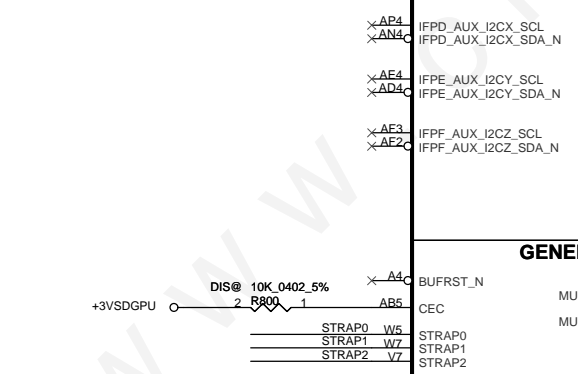
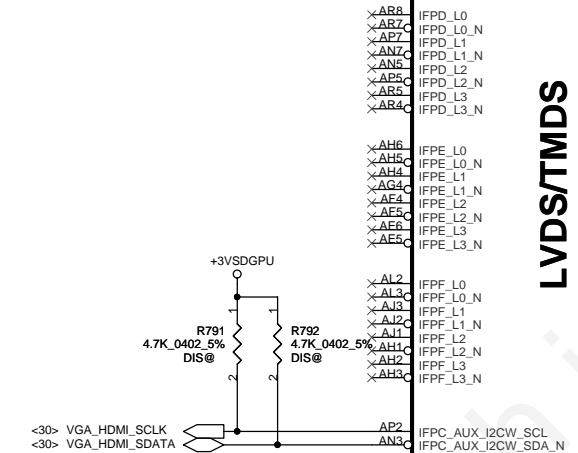
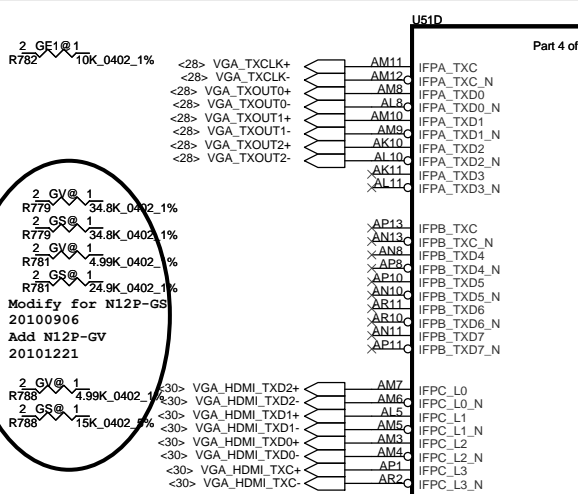
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Size Custom	Document Number 4019C0
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Mode E Command Mapping GB2-128 Package Femi	Mode C Command Mapping GB1-128 Package	Data Bit	
Fbx_CMD3	Fbx_CMD0	CKE_L	
Fbx_CMD8	Fbx_CMD1	A8	A8
Fbx_CMD2	Fbx_CMD2	CS0_L*	
Fbx_CMD21	Fbx_CMD3	A7	A6
Fbx_CMD24	Fbx_CMD4	A2	A1
Fbx_CMD23	Fbx_CMD5	A11	A9
Fbx_CMD26	Fbx_CMD6	A5	A4
Fbx_CMD7	Fbx_CMD7	A0	A12
Fbx_CMD15	Fbx_CMD8	CAS*	CAS*
Fbx_CMD13	Fbx_CMD9	BA1	A3
Fbx_CMD4	Fbx_CMD10	A9	A11
Fbx_CMD18	Fbx_CMD11	CS0_H	
Fbx_CMD29	Fbx_CMD12	BA0	BA0
Fbx_CMD27	Fbx_CMD13	BA2	A15
Fbx_CMD6	Fbx_CMD14	A3	BA1
Fbx_CMD17	Fbx_CMD15	CS1_H	
Fbx_CMD19	Fbx_CMD16	ODT_H	
Fbx_CMD22	Fbx_CMD17	A4	A5
Fbx_CMD12	Fbx_CMD18	A13	A14
Fbx_CMD28	Fbx_CMD19	WE*	A10
Fbx_CMD10	Fbx_CMD20	A1	A2
Fbx_CMD25	Fbx_CMD21	A10	WE*
Fbx_CMD9	Fbx_CMD22	A12	A0
Fbx_CMD1	Fbx_CMD23	CS1_L*	
Fbx_CMD11	Fbx_CMD24	RAS*	RAS*
Fbx_CMD0	Fbx_CMD25	ODT_L	
Fbx_CMD5	Fbx_CMD26	A6	A7
Fbx_CMD16	Fbx_CMD27	CKE_H	
Fbx_CMD20	Fbx_CMD28	RST	RST
Fbx_CMD14	Fbx_CMD29	A14	A13
Fbx_CMD30	Fbx_CMD30	A15	BA2
Fbx_CMD31			

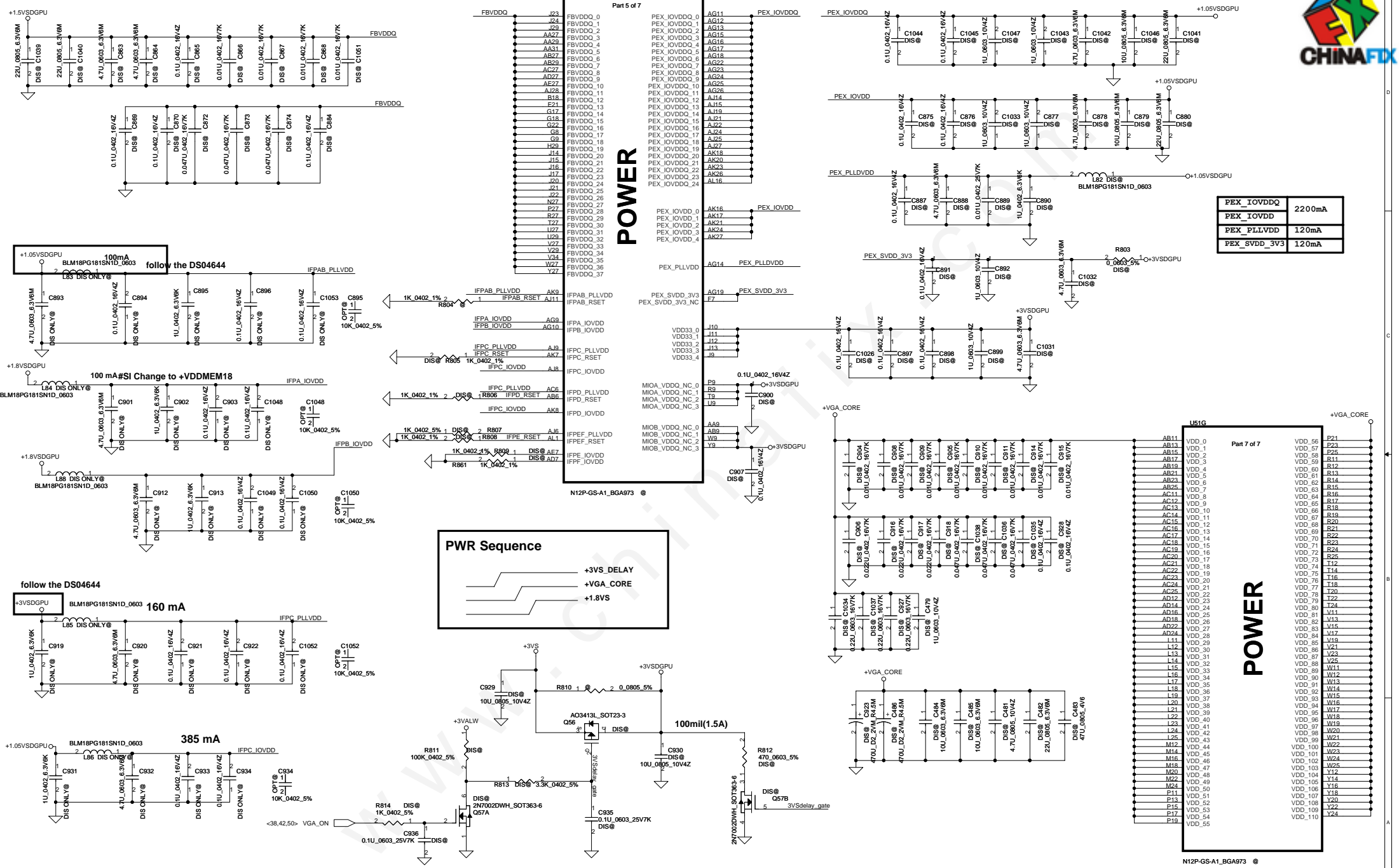
LOW HIGH



20091214 Modify For N11P-GV2H	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK		
64MX16 Samsung:SA000035720	H 45K	H 35K	H 30K	L 20K	L 10K	L 15K		
64MX16 Hynix:SA000032490	H 45K	H 35K	H 30K	L 15K	L 10K	L 15K		
20100113 Modify For N11P-GE1	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK		
64MX16 Samsung:SA000035720	H 45K	H 35K	H 10K	L 20K	L 10K	L 15K		
64MX16 Hynix:SA000032490	H 45K	H 35K	H 10K	L 15K	L 10K	L 15K		
20100601 Modify For N11P-GE	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK		
64MX16 Samsung:SA000035720	H 45K	L 35K	L 10K	L 20K	L 10K	H 15K		
64MX16 Hynix:SA000032490	H 45K	L 35K	L 10K	L 15K	L 10K	H 15K		
128MX16 Samsung:SA00003MQ40	H 45K	L 35K	L 10K	L 45K	L 10K	H 15K		
128MX16 Hynix:SA00003VS10	H 45K	L 35K	L 10K	L 35K	L 10K	H 15K		
20100909 Modify For N12P-GS VRAM: DDR3 900 down to 800	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
64MX16 (800) Samsung:SA000035720	H 45K	H 35K	L 25K	NC	NC	L 10K	L 10K	H 15K
64MX16 (800) Hynix:SA000032490	H 45K	H 35K	L 25K	NC	NC	L 5K	L 10K	H 15K
64MX16 (900) Samsung:K4W1G1646G-BC11 SA00004GS10	H 45K	L 35K	L 25K	NC	NC	L 20K	L 10K	H 15K
64MX16 (900) Hynix:HTQ1G63DFR-11C SA000041S40	H 45K	L 35K	L 25K	NC	NC	L 15K	L 10K	H 15K
128MX16 (800) Samsung:SA00003MQ40	H 45K	H 35K	L 25K	NC	NC	L 45K	L 10K	H 15K
128MX16 (800) Hynix:SA00003VS10	H 45K	H 35K	L 25K	NC	NC	L 35K	L 10K	H 15K
128MX16 (900) Samsung:K4W2G1646C-HC11 SA000047Q20	H 45K	L 35K	L 25K	NC	NC	L 45K	L 10K	H 15K
128MX16 (900) Hynix:HTQ2G63BFR-11C SA00003YQ20	H 45K	L 35K	L 25K	NC	NC	L 35K	L 10K	H 15K
20101220 Modify For N12P-GV-OP VRAM: DDR3 900 down to 800	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
64MX16 (900) Samsung:K4W1G1646G-BC11 SA00004GS10	H 45K	L 35K	L 5K	L 5K	L 10K	L 20K	H 10K	H 5K
64MX16 (900) Hynix:HTQ1G63DFR-11C SA000041S40	H 45K	L 35K	L 5K	L 5K	L 10K	L 15K	L 10K	H 5K
128MX16 (900) Samsung:K4W2G1646C-HC11 SA000047Q20	H 45K	L 35K	L 5K	L 5K	L 10K	L 45K	L 10K	H 5K
128MX16 (900) Hynix:HTQ2G63BFR-11C SA00003YQ20	H 45K	L 35K	L 5K	L 5K	L 10K	L 35K	L 10K	H 5K

ROM_SI, 爲Vram配打電阻

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								Size		Document Number				Rev	
								Custom		4019CO					
								Date:		Thursday, January 20, 2011				Sheet 23 of 56	



POWER



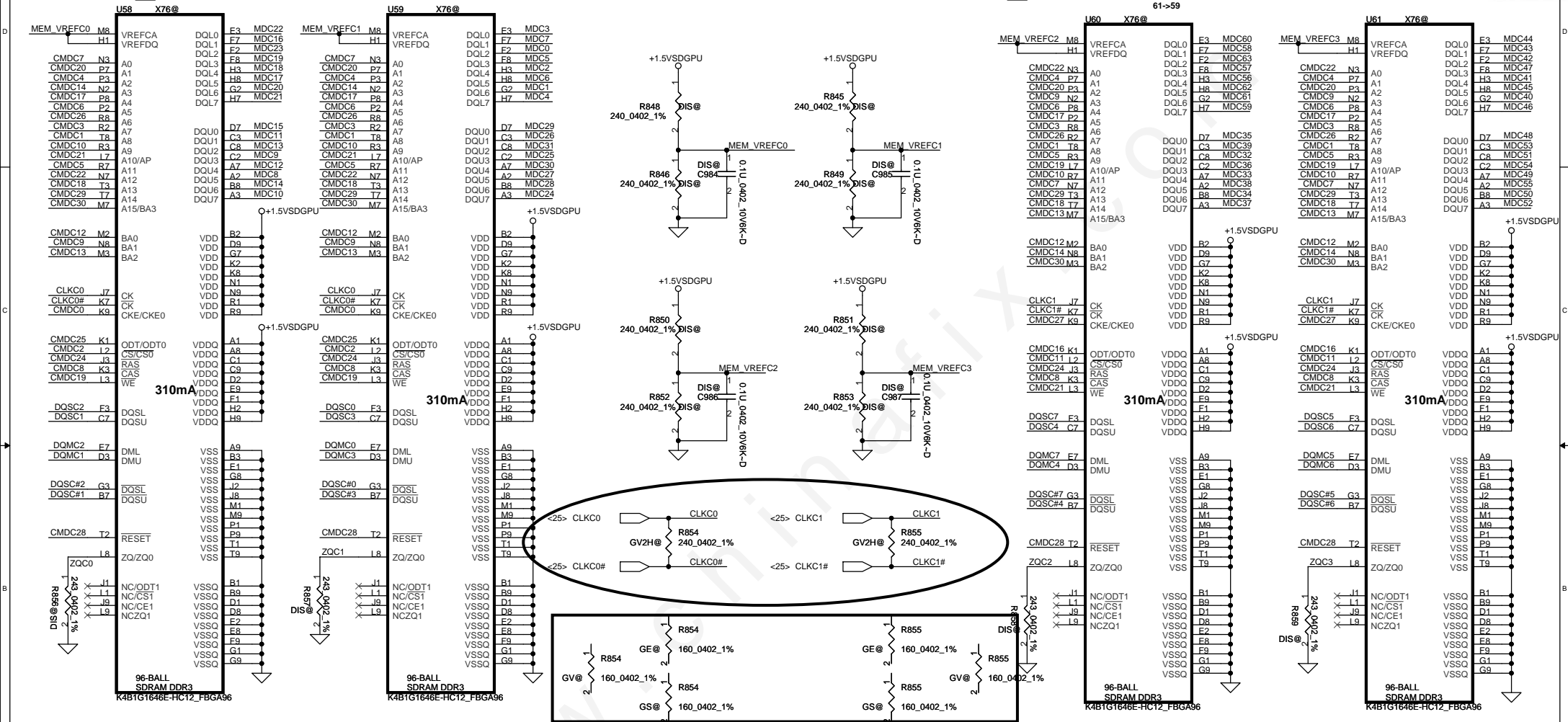


<25> DQSC[7..0] DQSC[7..0]
<25> DQSC#[7..0] DQSC#[7..0]
<25> DQMC[7..0] DQMC[7..0]
<25> MDC[63..0] MDC[63..0]
<25> CMDC[30..0] CMDC[30..0]

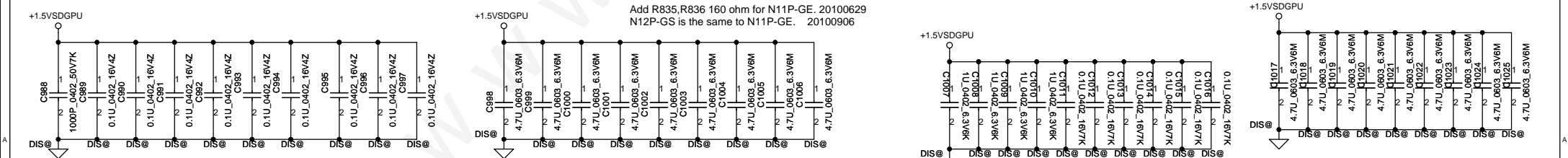
MODE C PULL DOWN SIGNAL: RST, CKE, ODT

<25> DQMC[7..0] DQMC[7..0]
<25> CMDC[30..0] CMDC[30..0]
<25> DQSC[7..0] DQSC[7..0]
<25> DQSC#[7..0] DQSC#[7..0]
<25> MDC[63..0] MDC[63..0]

U60 RAM BIT SWAP 20091211
60->60
62->58
58->63
63->57
59->56
56->62
57->61
61->59

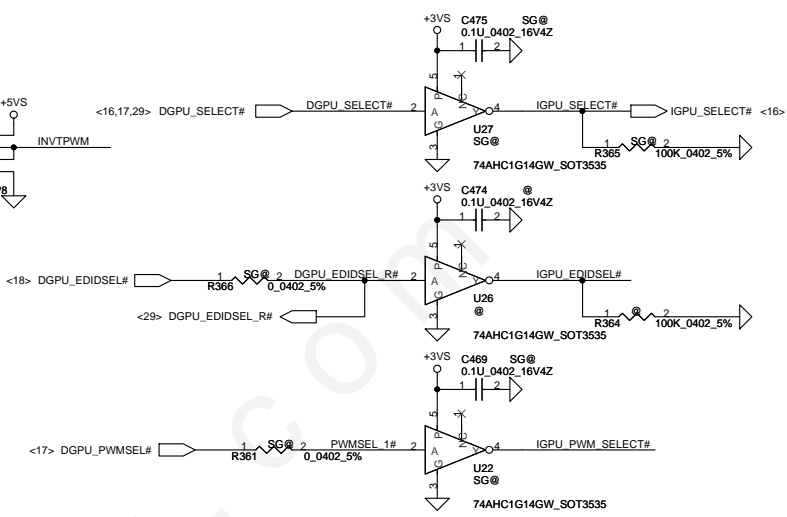
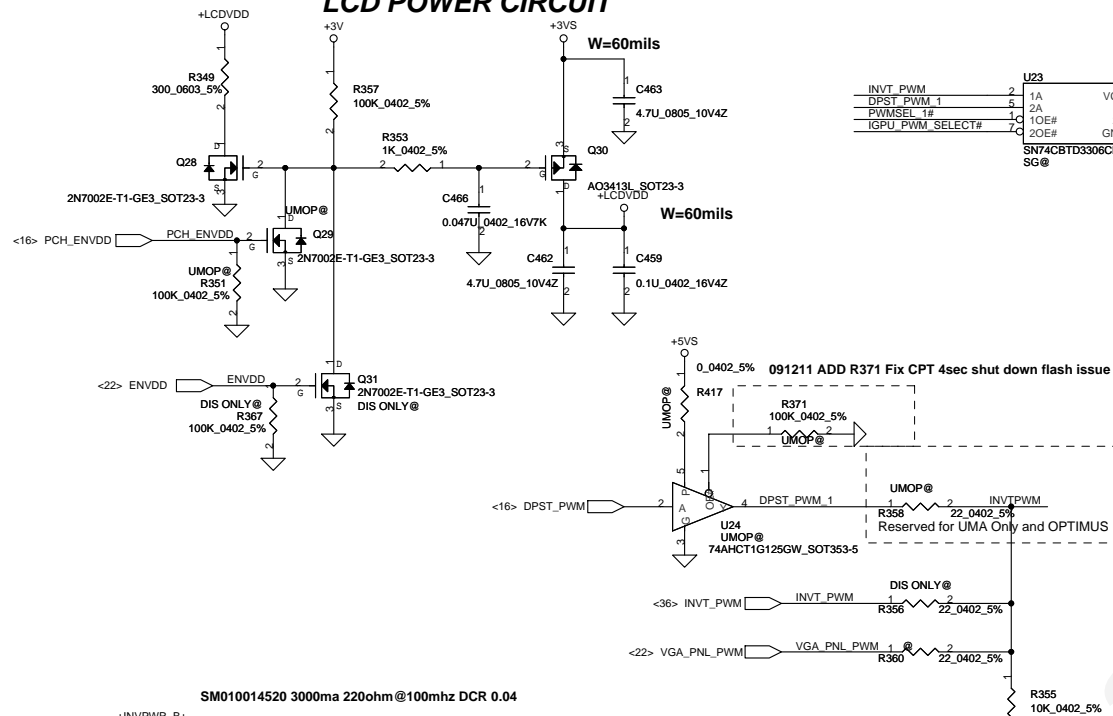


Add R835, R836 160 ohm for N11P-GE. 20100629
N12P-GS is the same to N11P-GE. 20100906

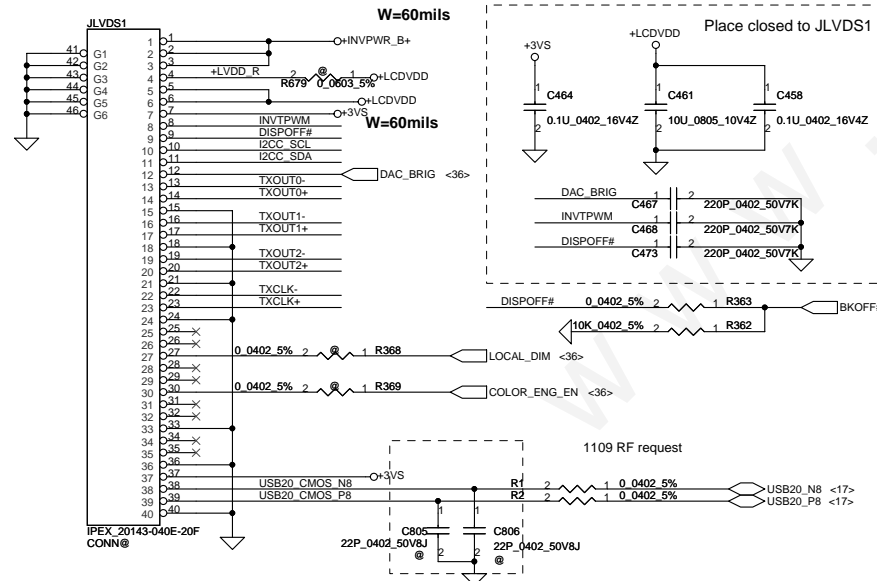


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				Custom	4019CO	
				Date:	Thursday, January 20, 2011	Sheet 27 of 56

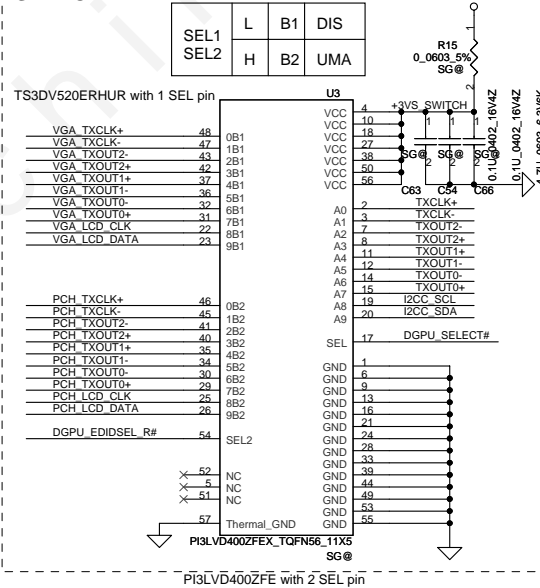
LCD POWER CIRCUIT



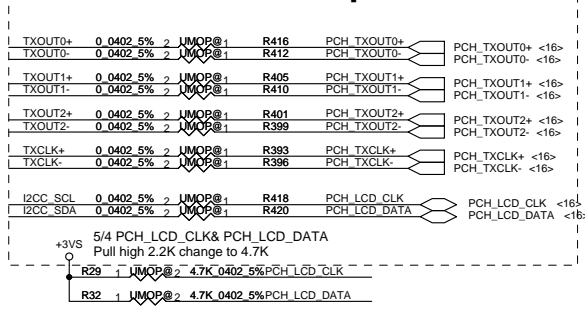
LCD/LED PANEL Conn.



SWITCHABLE



UMA ONLY / Optimus



Discrete ONLY



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Date: Thursday, January 20, 2011				Sheet	28 of 56

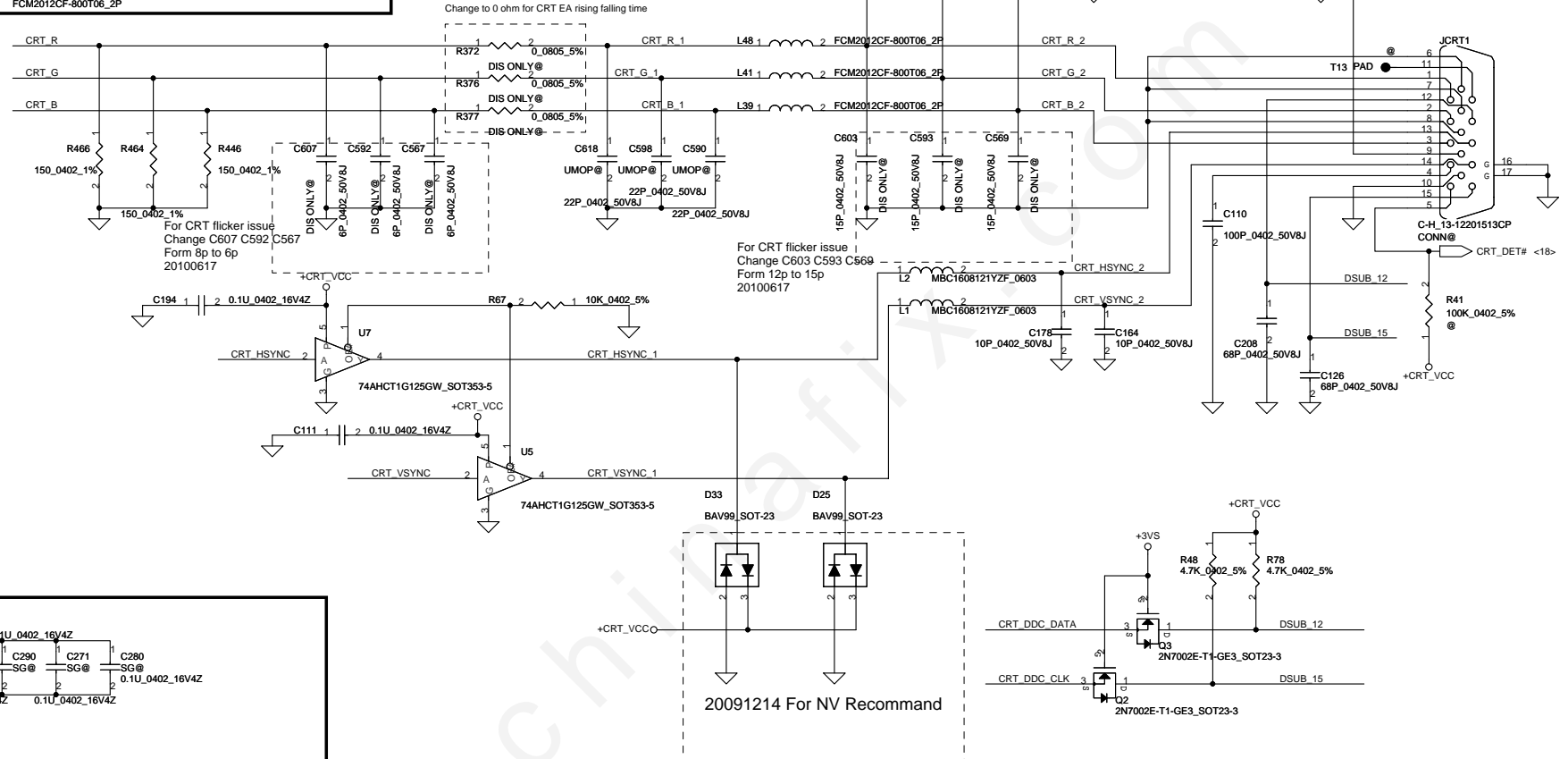


UMA ONLY & OPTIMUS

UMOP@ C607 1/2 UMOP@ C592 1/2 UMOP@ C567 1/2
10P_0402_50V8J 10P_0402_50V8J 10P_0402_50V8J

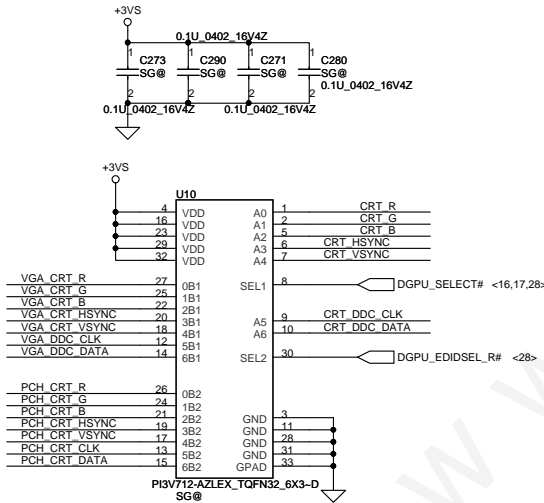
R372 UMOP@
1 FCM2012CF-800T06_2P
R376 UMOP@
1 FCM2012CF-800T06_2P
R377 UMOP@
1 FCM2012CF-800T06_2P

UMOP@ C603 1/2 UMOP@ C593 1/2 UMOP@ C569 1/2
10P_0402_50V8J 10P_0402_50V8J 10P_0402_50V8J



SWITCHABLE

2009/08/27



L	B1	DIS
H	B2	UMA

Discrete only

<22>	VGA_CRT_R	VGA_CRT_R	R537	DIS ONLY@	0.0402_5%	CRT_R
<22>	VGA_CRT_G	VGA_CRT_G	R535	DIS ONLY@	0.0402_5%	CRT_G
<22>	VGA_CRT_B	VGA_CRT_B	R533	DIS ONLY@	0.0402_5%	CRT_B
<22>	VGA_CRT_HSYNC	VGA_CRT_HSYNC	R531	DIS ONLY@	0.0402_5%	CRT_HSYNC
<22>	VGA_CRT_VSYNC	VGA_CRT_VSYNC	R529	DIS ONLY@	0.0402_5%	CRT_VSYNC
<22>	VGA_DDC_CLK	VGA_DDC_CLK	R527	DIS ONLY@	0.0402_5%	CRT_DDC_CLK
<22>	VGA_DDC_DATA	VGA_DDC_DATA	R526	DIS ONLY@	0.0402_5%	CRT_DDC_DATA

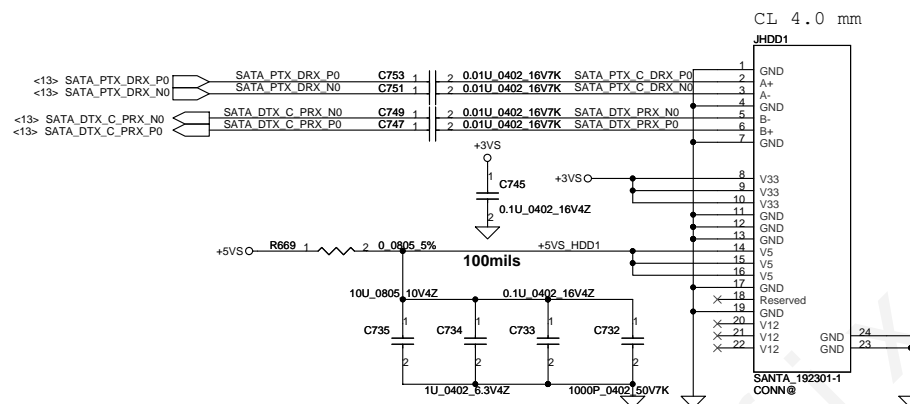
VGA_DDC_DATA and VGA_DDC_CLK Pull high at Page22

UMA only & Optimus

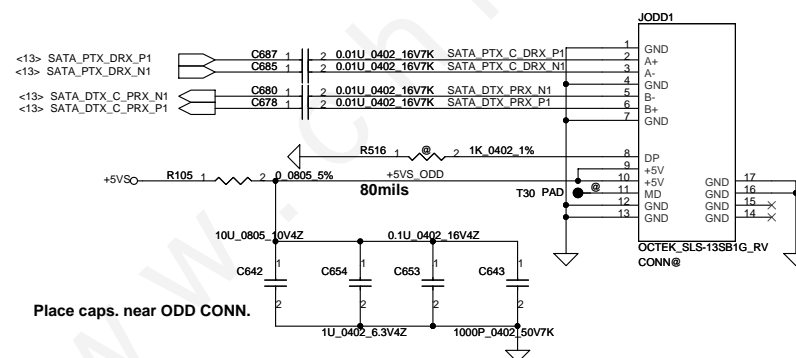
<16>	PCH_CRT_R	PCH_CRT_R	R536	UMOP@	0.0402_5%	CRT_R
<16>	PCH_CRT_G	PCH_CRT_G	R534	UMOP@	0.0402_5%	CRT_G
<16>	PCH_CRT_B	PCH_CRT_B	R532	UMOP@	0.0402_5%	CRT_B
<16>	PCH_CRT_HSYNC	PCH_CRT_HSYNC	R530	UMOP@	0.0402_5%	CRT_HSYNC
<16>	PCH_CRT_VSYNC	PCH_CRT_VSYNC	R528	UMOP@	0.0402_5%	CRT_VSYNC
<16>	PCH_CRT_CLK	PCH_CRT_CLK	R544	UMOP@	0.0402_5%	CRT_DDC_CLK
<16>	PCH_CRT_DATA	PCH_CRT_DATA	R543	UMOP@	0.0402_5%	CRT_DDC_DATA

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Date: Thursday, January 20, 2011				Sheet 29 of 56

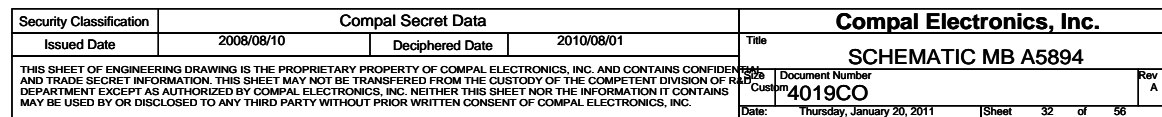
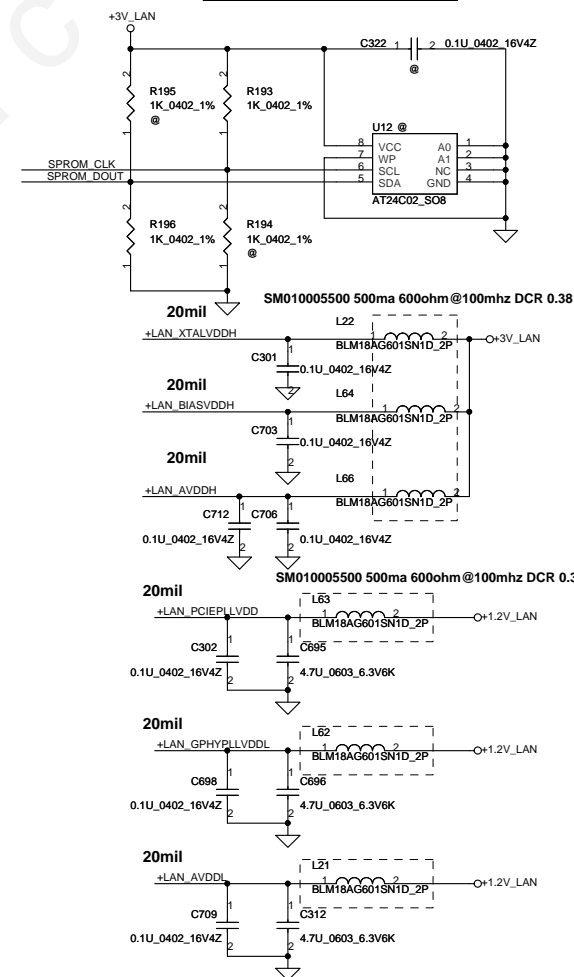
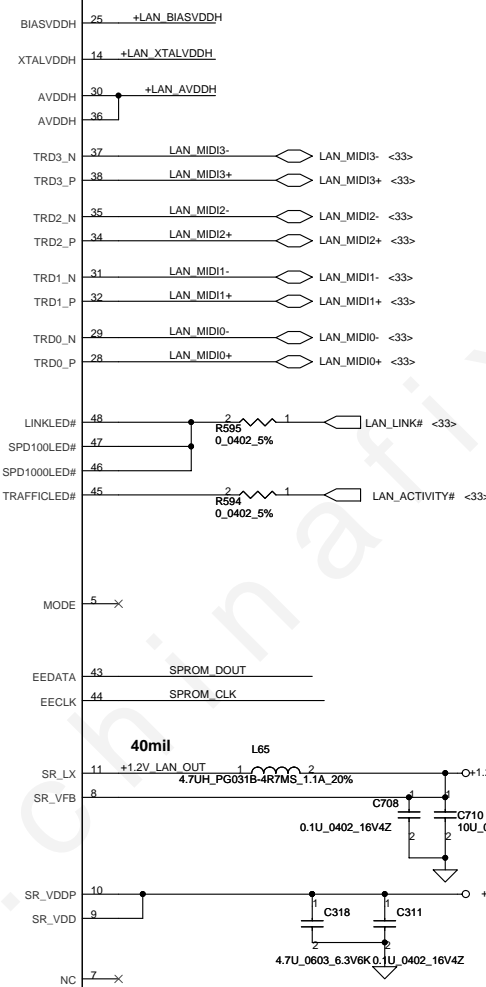
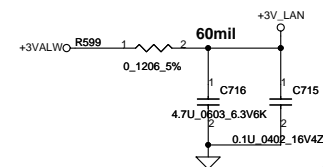
SATA HDD1 Conn.



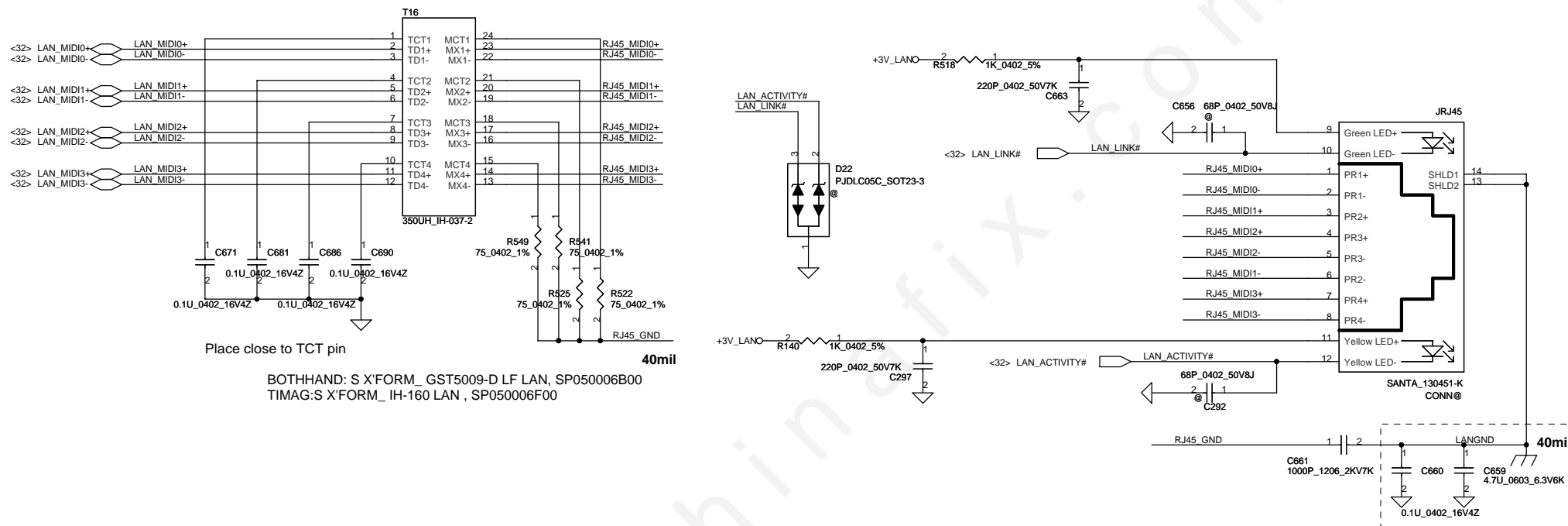
SATA ODD Conn.



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				Date:	Thursday, January 20, 2011
				Sheet	31 of 56

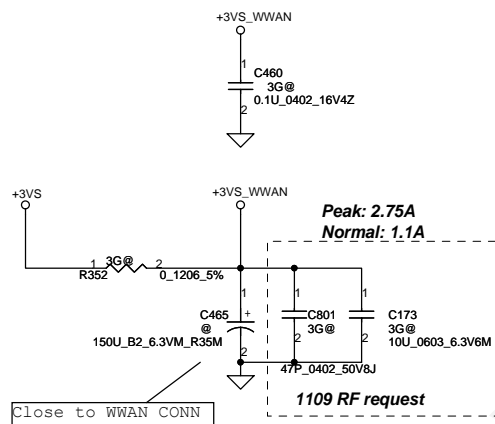
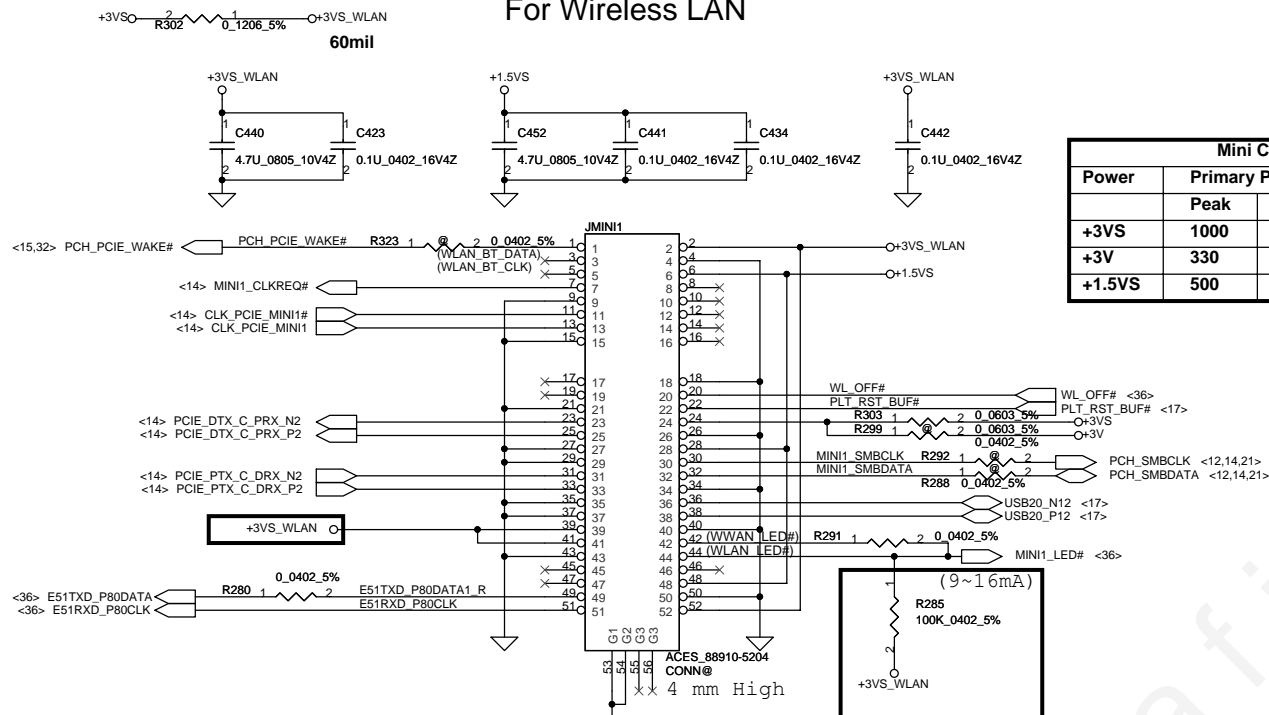


LAN Connector



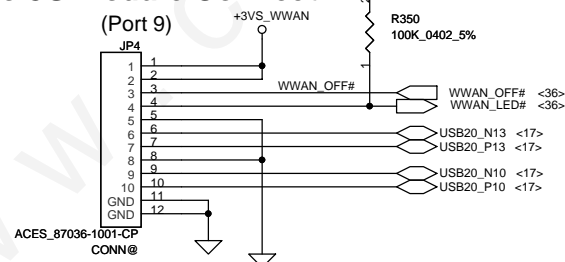
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				Date	Thursday, January 20, 2011
				Sheet	33 of 56

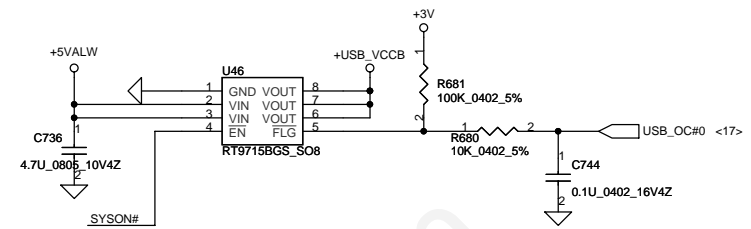
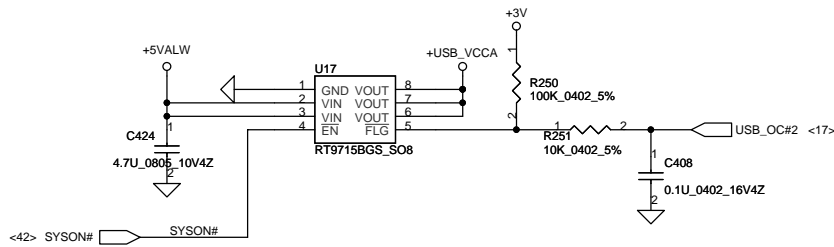
For Wireless LAN



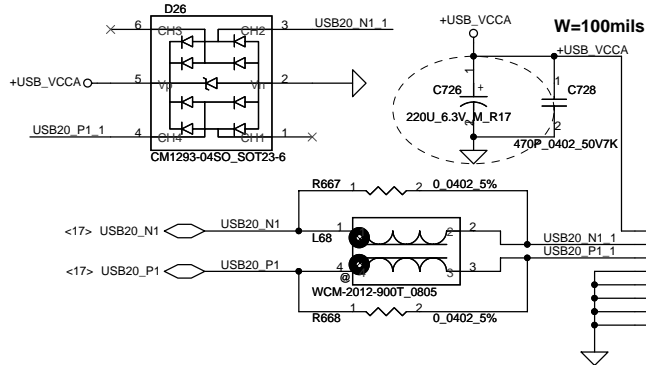
For 3G / GPS To 3G Module Connect

LS-5895





2009/08/14 CHANGE cap



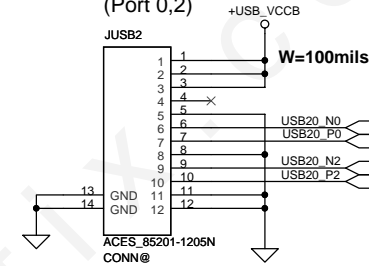
2009/08/25 Update Footprint(follow NAL00)

USB Conn.
(Port 1)

SUYIN_020133GB004M51PZR
CONN@

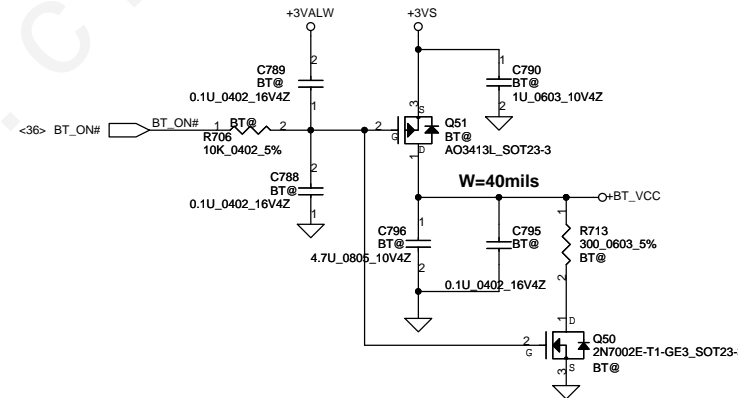
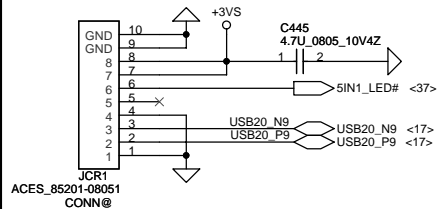
USB/B Conn. LS-5891

(Port 0,2)



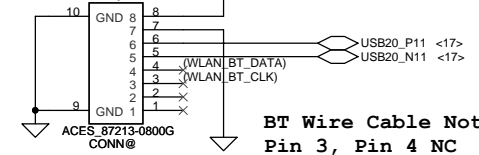
2009/08/24 CHANGE Conn to FFC Type

Card Reader Conn. LS-5896



BT Conn.

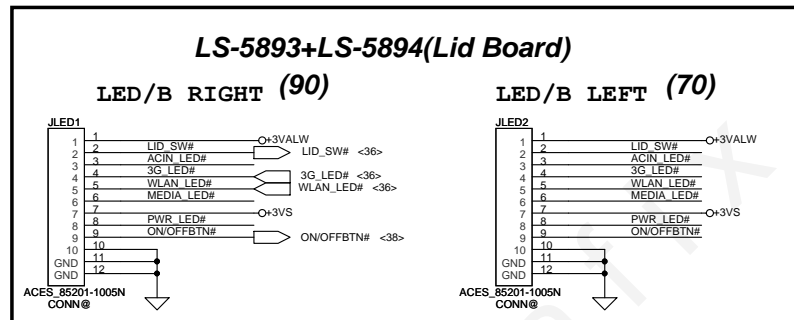
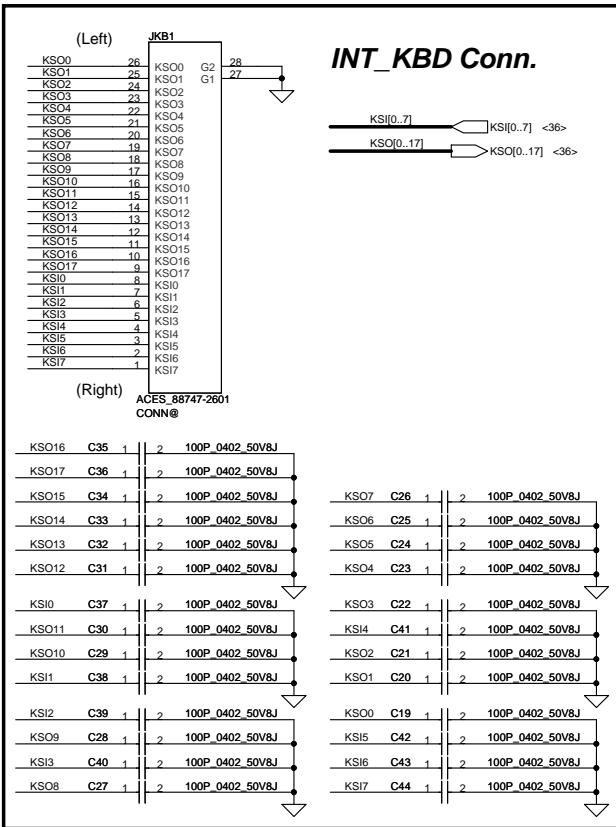
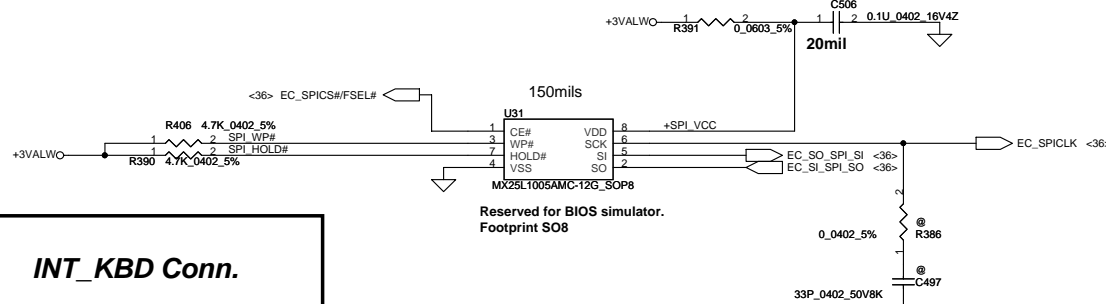
(Port 11)



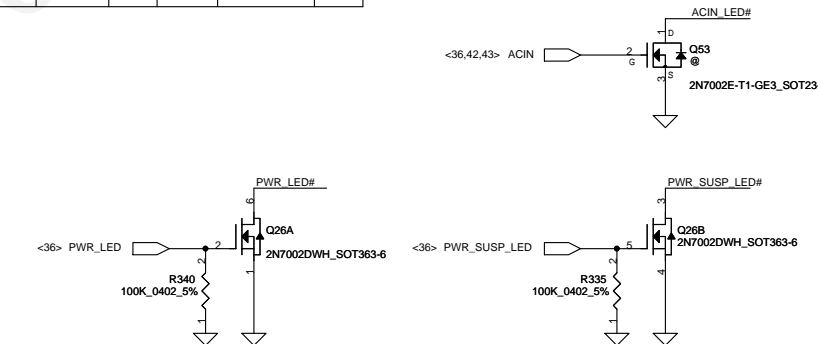
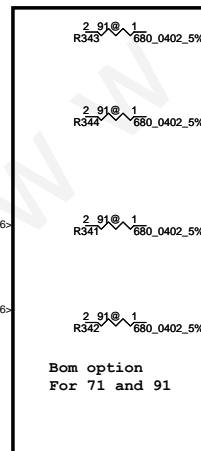
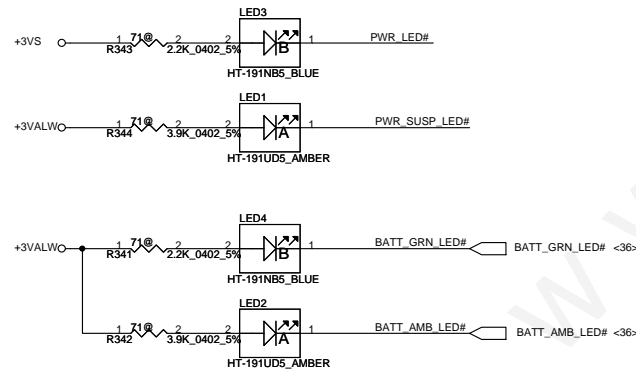
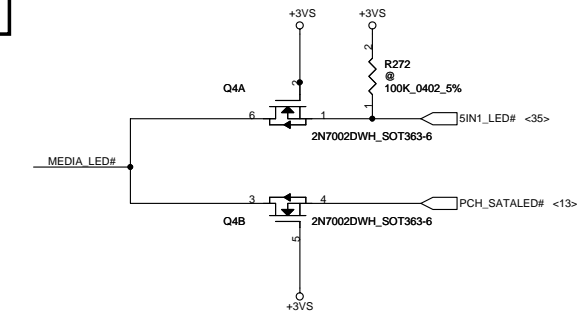
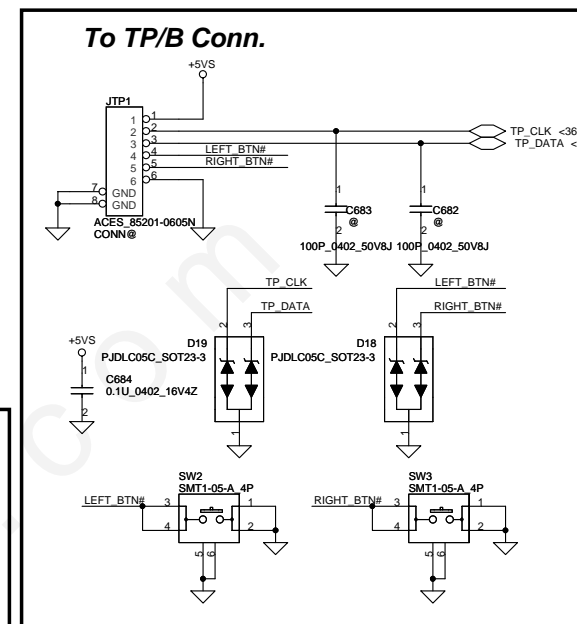
BT Wire Cable Note:
Pin 3, Pin 4 NC

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				Custom	4019CO
				Date	Thursday, January 20, 2011
				Sheet	35 of 56





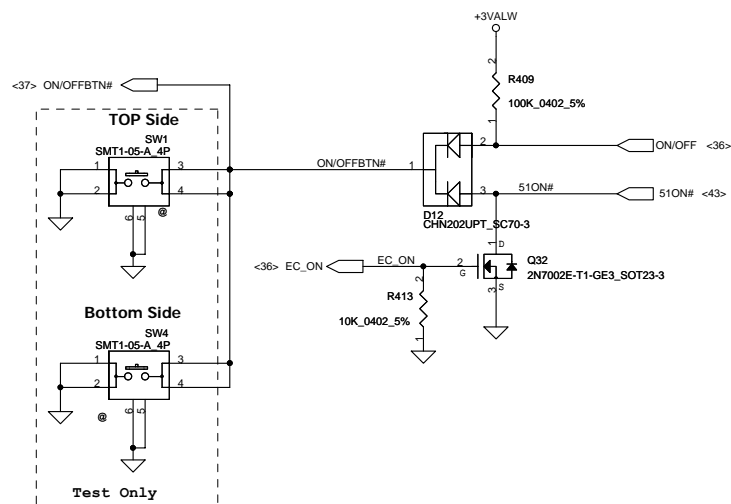
LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		



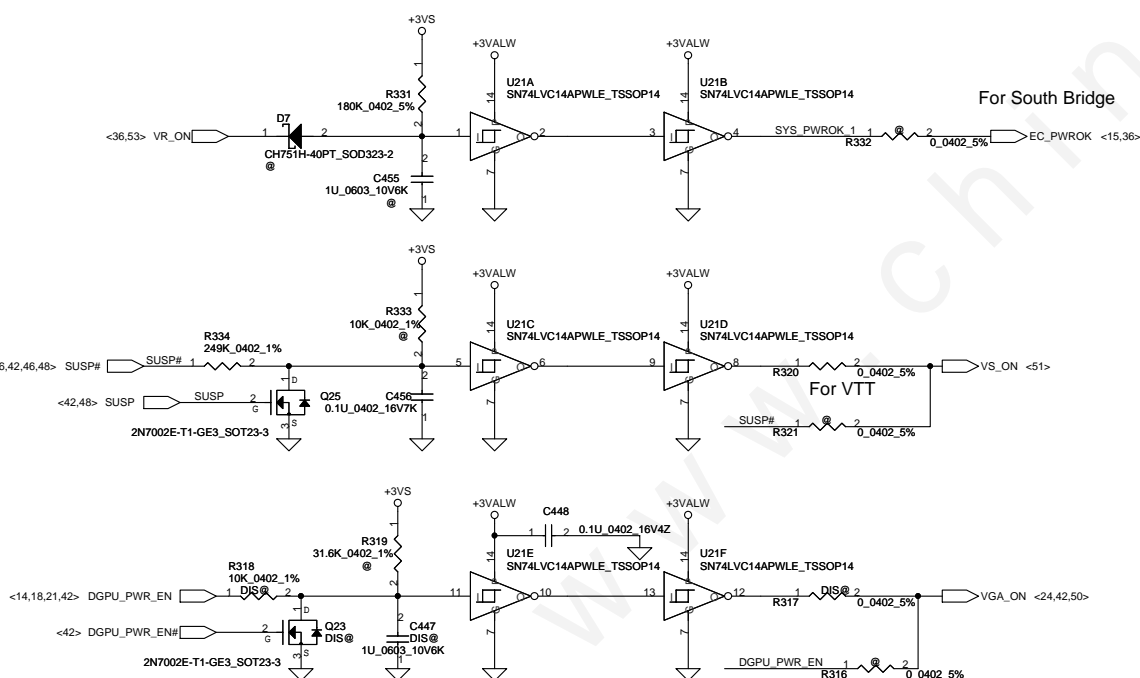
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				Date	Thursday, January 20, 2011
				Sheet	37 of 56

Power Button

ON/OFF switch



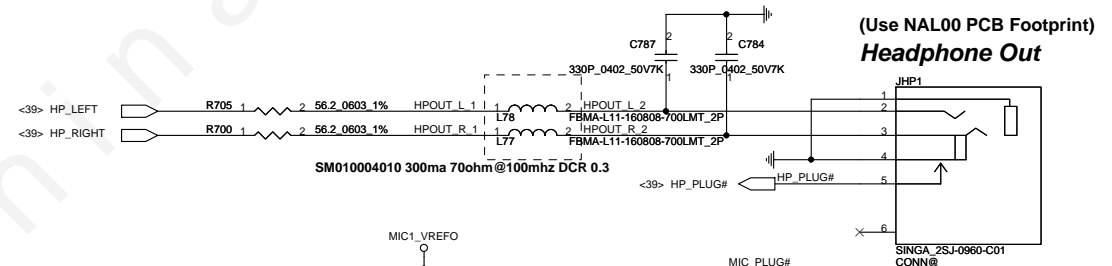
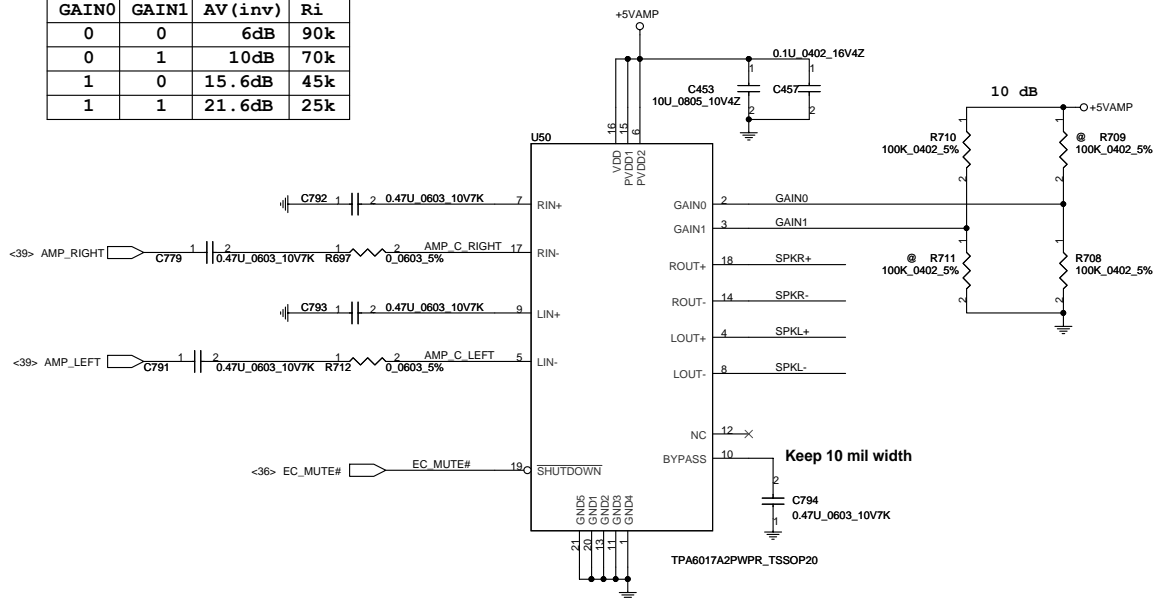
Power ON Circuit



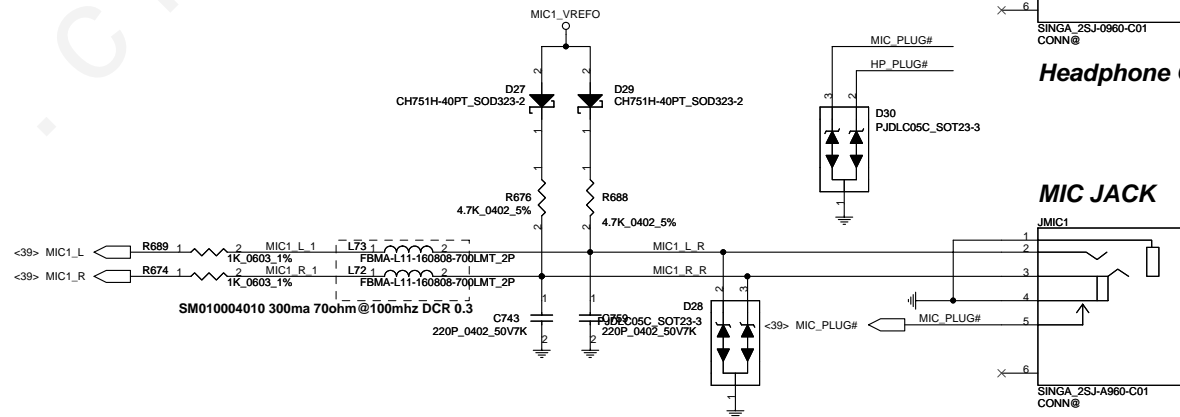
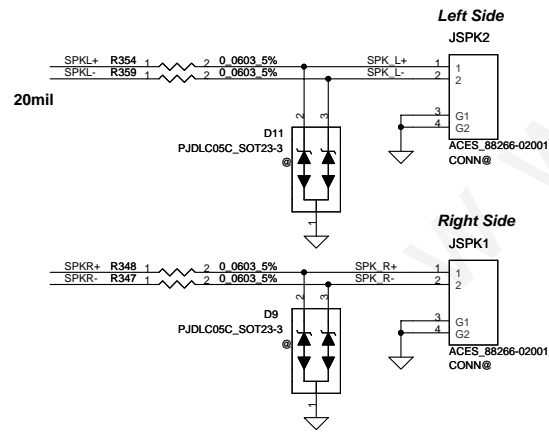
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Issued Date				2008/08/10				Deciphered Date			
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				Document Number				4019CO			
				Date				Thursday, January 20, 2011			
				Sheet				38 of 56			



GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

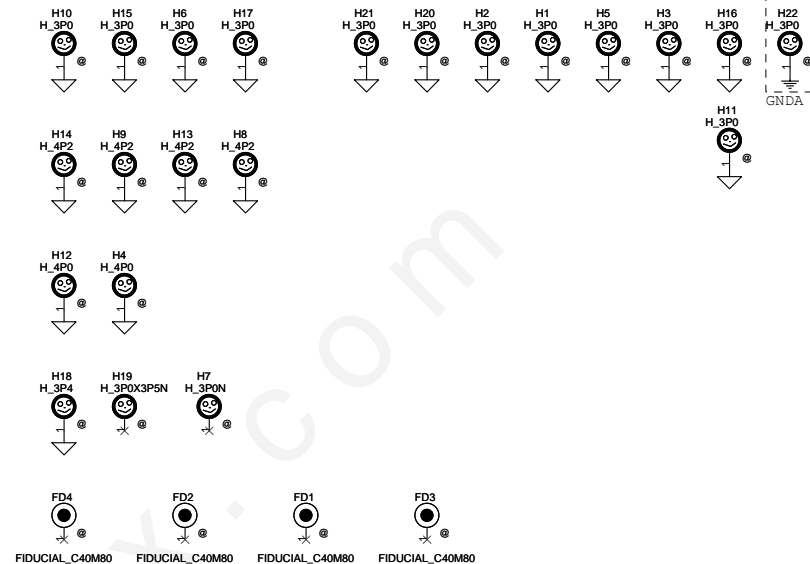
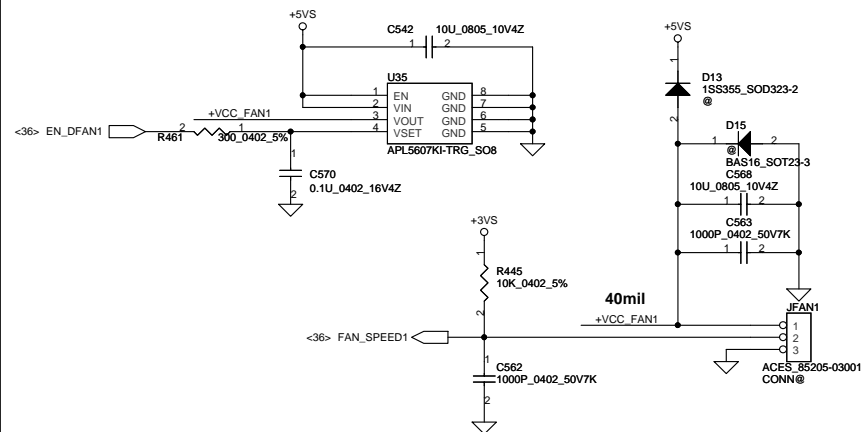


Int. Speaker Conn.

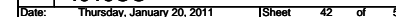


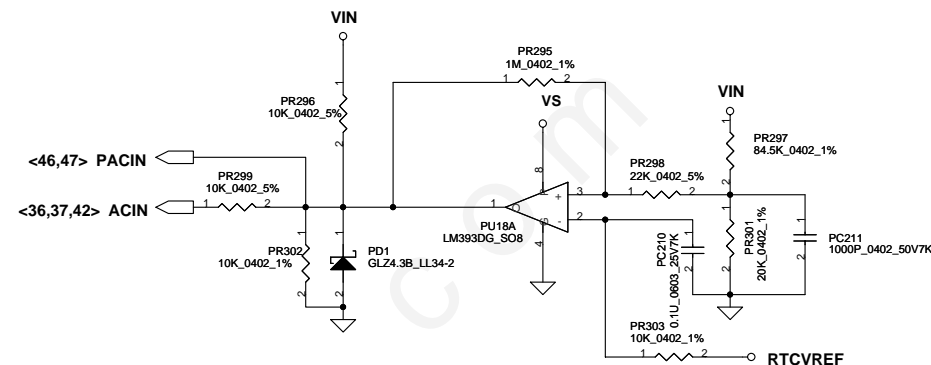
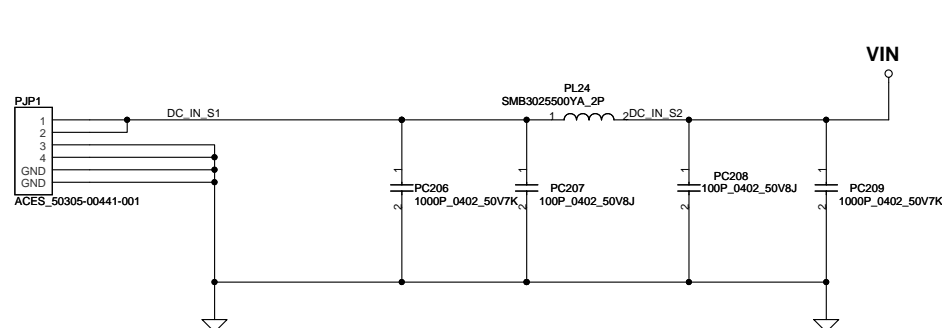
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				Document Number				4019CO			
				Date				Thursday, January 20, 2011			
				Sheet				40 of 56			

FAN1 Conn



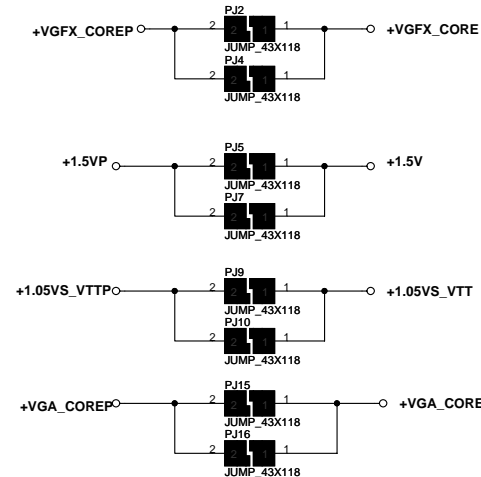
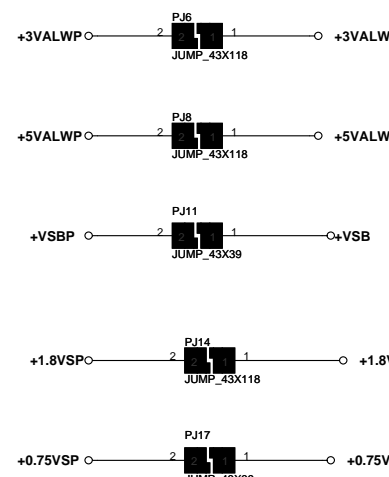
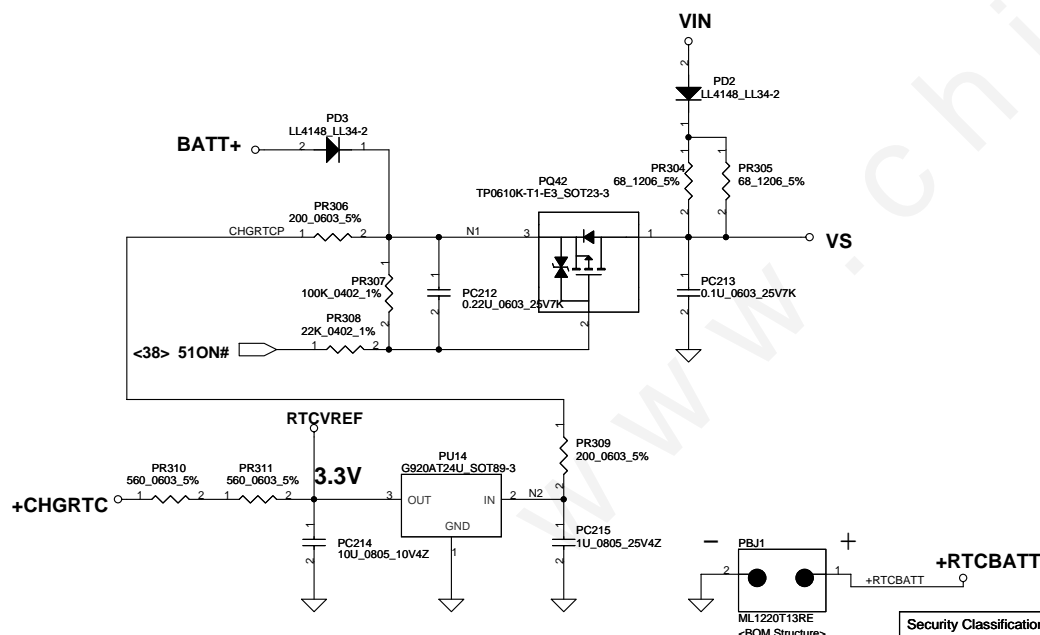
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				4019CO	
				Date: Thursday, January 20, 2011	Sheet 41 of 56



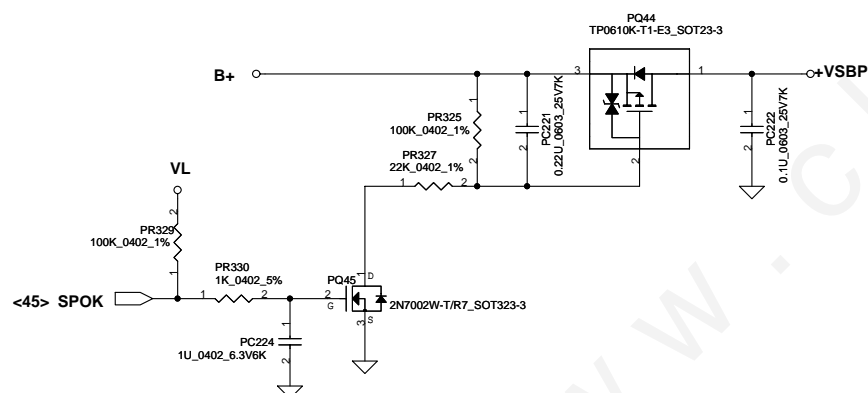
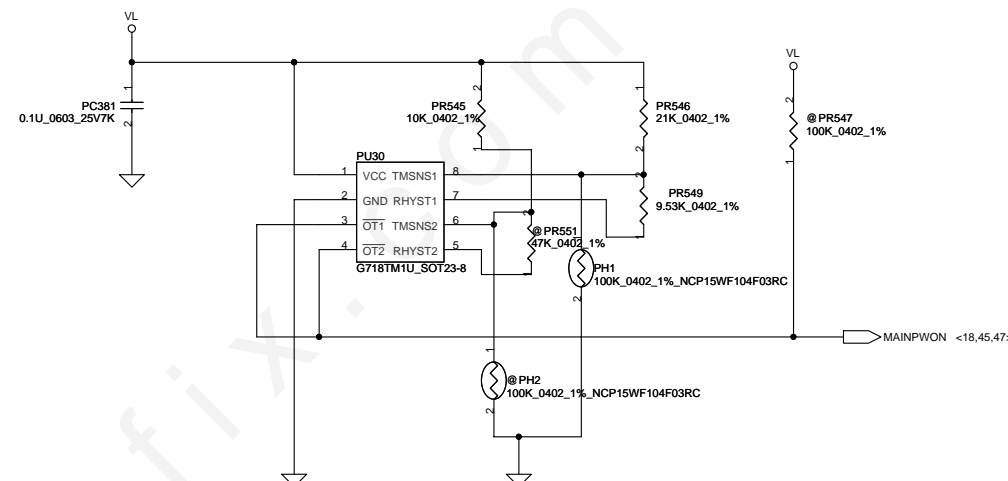
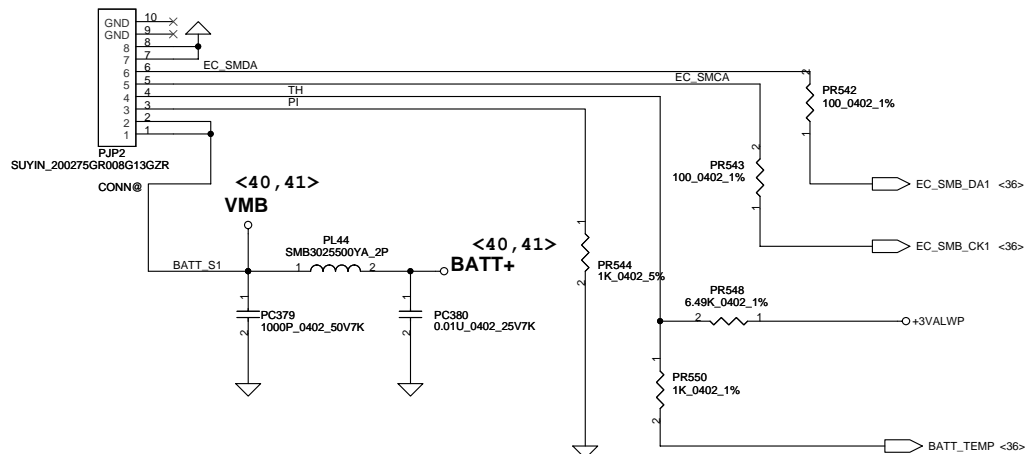


Vin Dectector

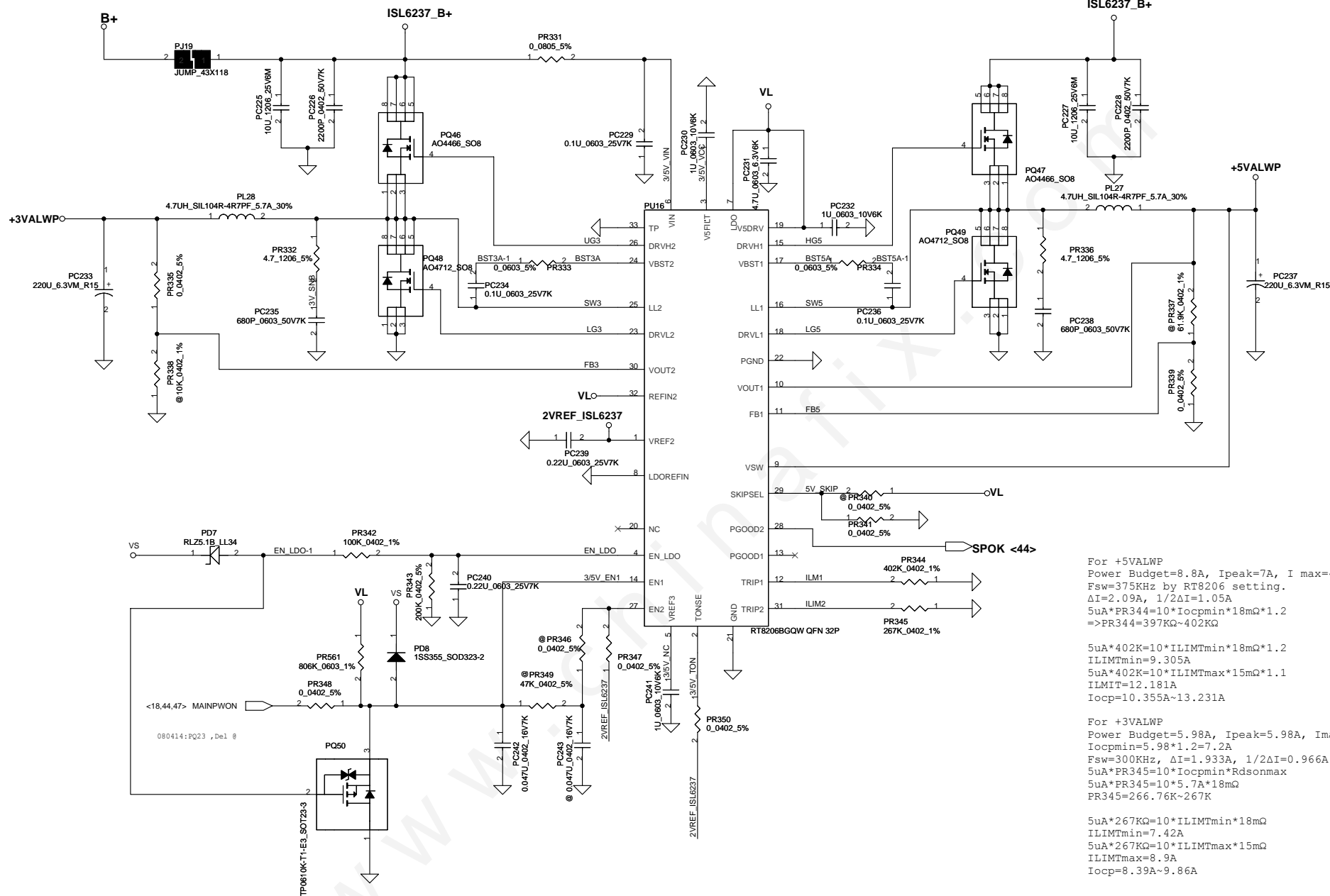
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



PH1 under CPU botten side :
CPU thermal protection at 92 degree C



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				Date	Thursday, January 20, 2011
				Sheet	44 of 56



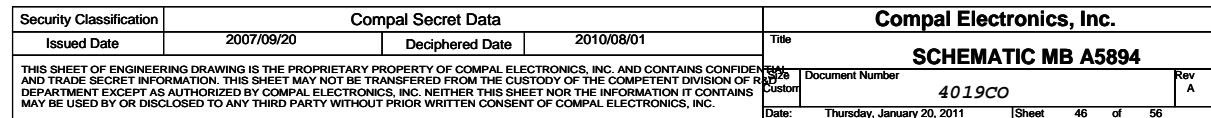
For +5VALWP
Power Budget=8.8A, I_{peak}=7A, I_{max}=4.9A
F_{sw}=375KHz by RT8206 setting.
 $\Delta I = 2.09A$, $1/2\Delta I = 1.05A$
 $5uA \cdot PR344 = 10 \cdot I_{ocpmin} \cdot 18m\Omega \cdot 1.2$
 $\Rightarrow PR344 = 397K\Omega \sim 402K\Omega$

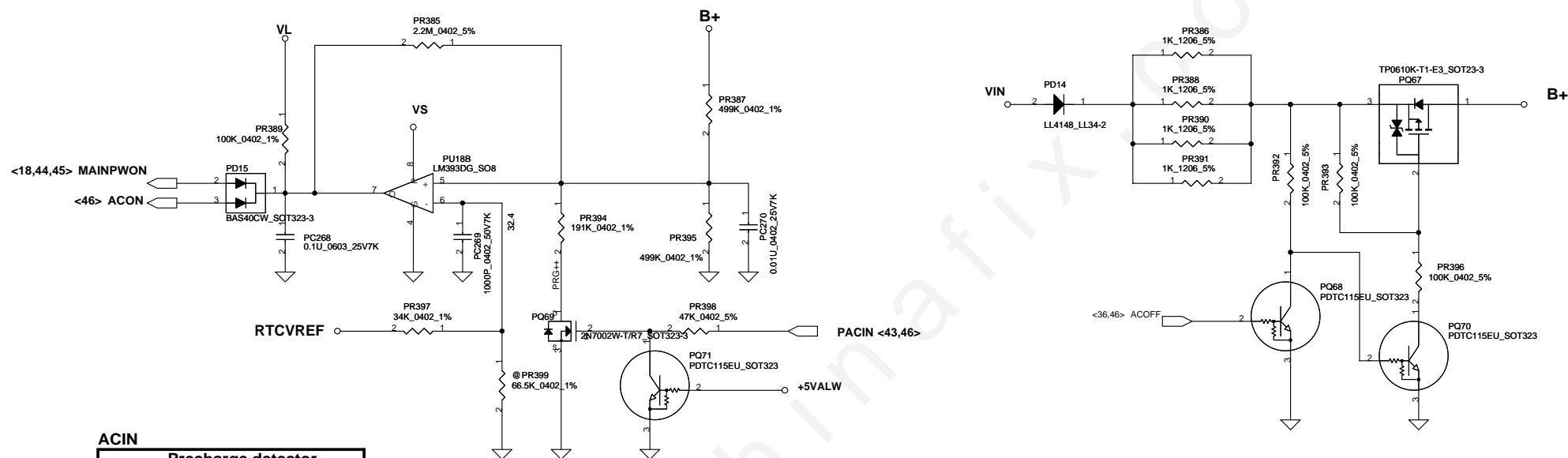
$5uA \cdot 402K = 10 \cdot ILIMITmin \cdot 18m\Omega \cdot 1.2$
 $ILIMITmin = 9.305A$
 $5uA \cdot 402K = 10 \cdot ILIMITmax \cdot 15m\Omega \cdot 1.1$
 $ILIMIT = 12.181A$
 $I_{ocp} = 10.355A \sim 13.231A$

For +3VALWP
Power Budget=5.98A, I_{peak}=5.98A, I_{max}=4.2A
 $I_{ocpmin} = 5.98 \cdot 1.2 = 7.2A$
F_{sw}=300KHz, $\Delta I = 1.933A$, $1/2\Delta I = 0.966A$
 $5uA \cdot PR345 = 10 \cdot I_{ocpmin} \cdot R_{dsonmax}$
 $5uA \cdot PR345 = 10 \cdot 5.7A \cdot 18m\Omega$
 $PR345 = 266.76K\Omega \sim 267K\Omega$

$5uA \cdot 267K\Omega = 10 \cdot ILIMITmin \cdot 18m\Omega$
 $ILIMITmin = 7.42A$
 $5uA \cdot 267K\Omega = 10 \cdot ILIMITmax \cdot 15m\Omega$
 $ILIMITmax = 8.9A$
 $I_{ocp} = 8.39A \sim 9.86A$

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				4019CO
Date: Thursday, January 20, 2011				Sheet 45 of 56





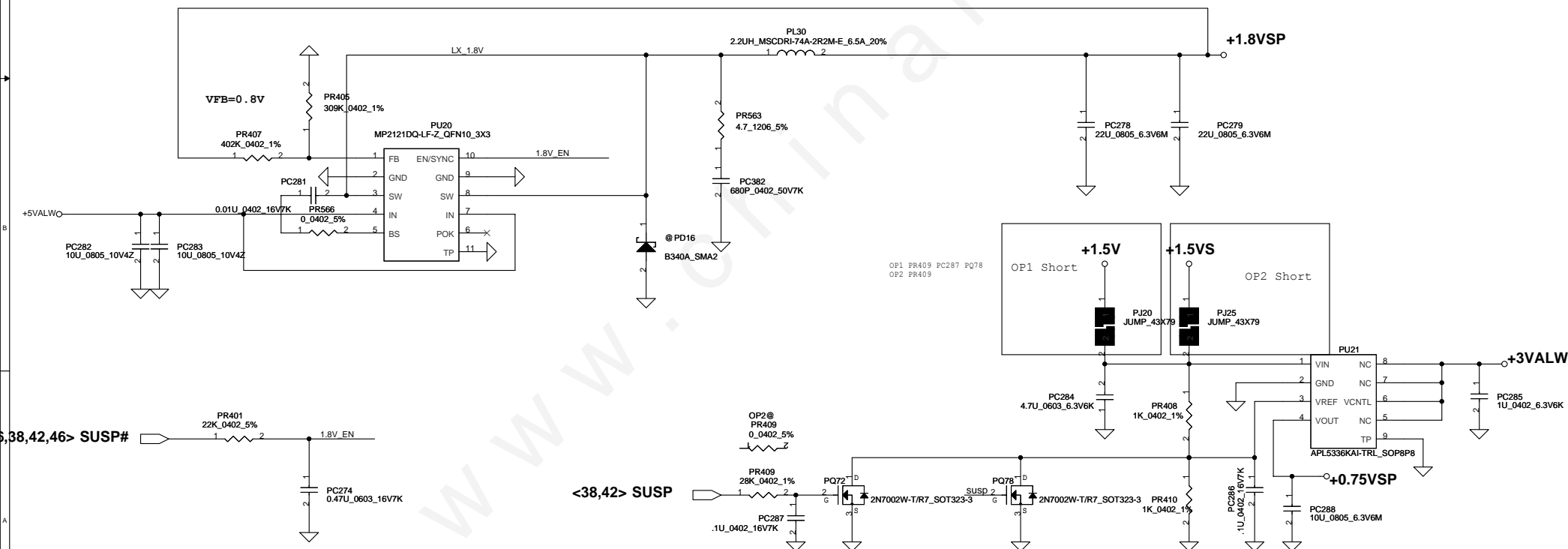
ACIN

	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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Title	SCHEMATIC MB A5894		Document Number	4019CO
Date:	Thursday, January 20, 2011		Sheet	47 of 56



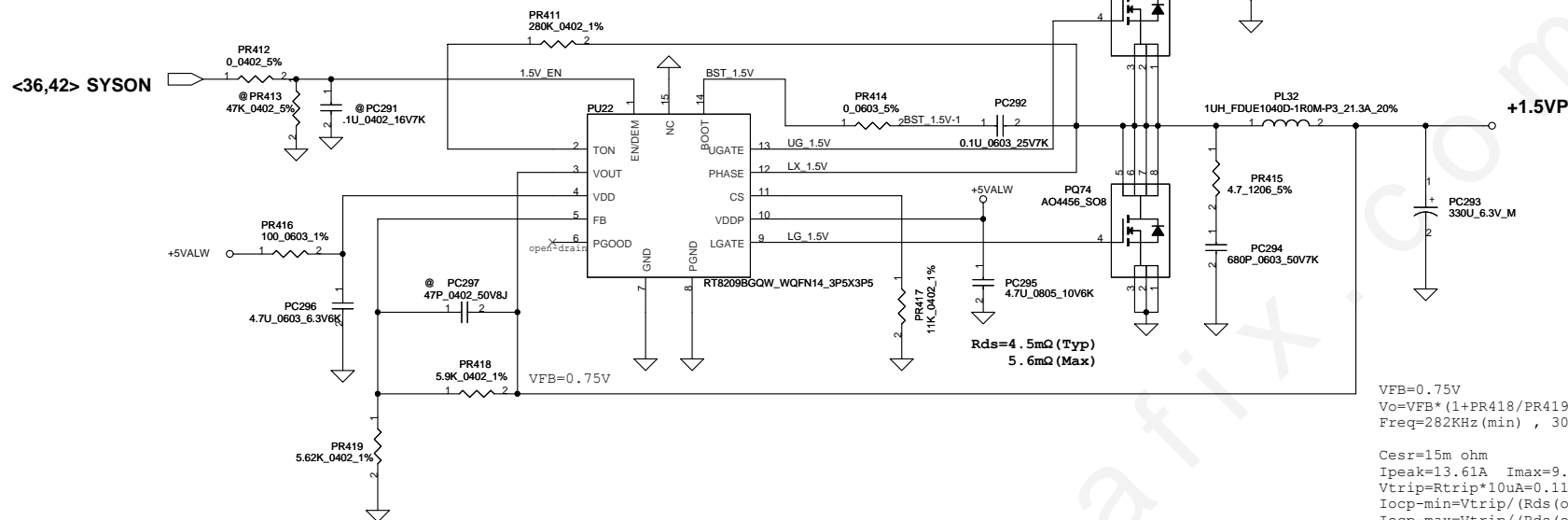
<38,42,46> SUSP#

<38,42> SUSP

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				4019CO
				Rev A
				Date: Thursday, January 20, 2011
				Sheet 48 of 56

EN_PSV
1. GND=>Disable SMPS
2. FLOAT=>PWM_only mode
3. HIGH=>Auto_skip mode

Because +1.5VSP has 17.74A power budget, it includes
DDR3, VGA chip, VRAM, so must use molding choke.

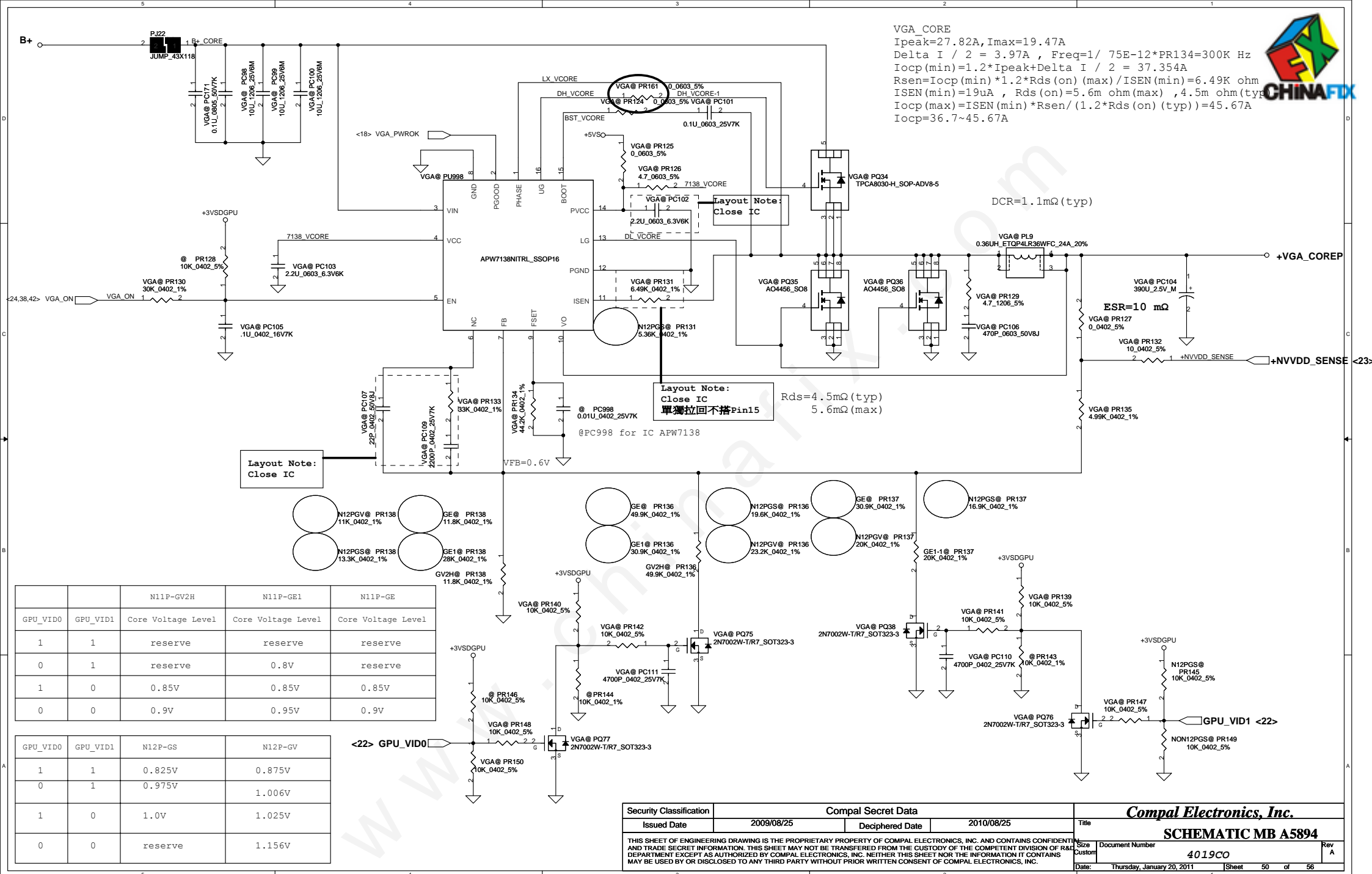


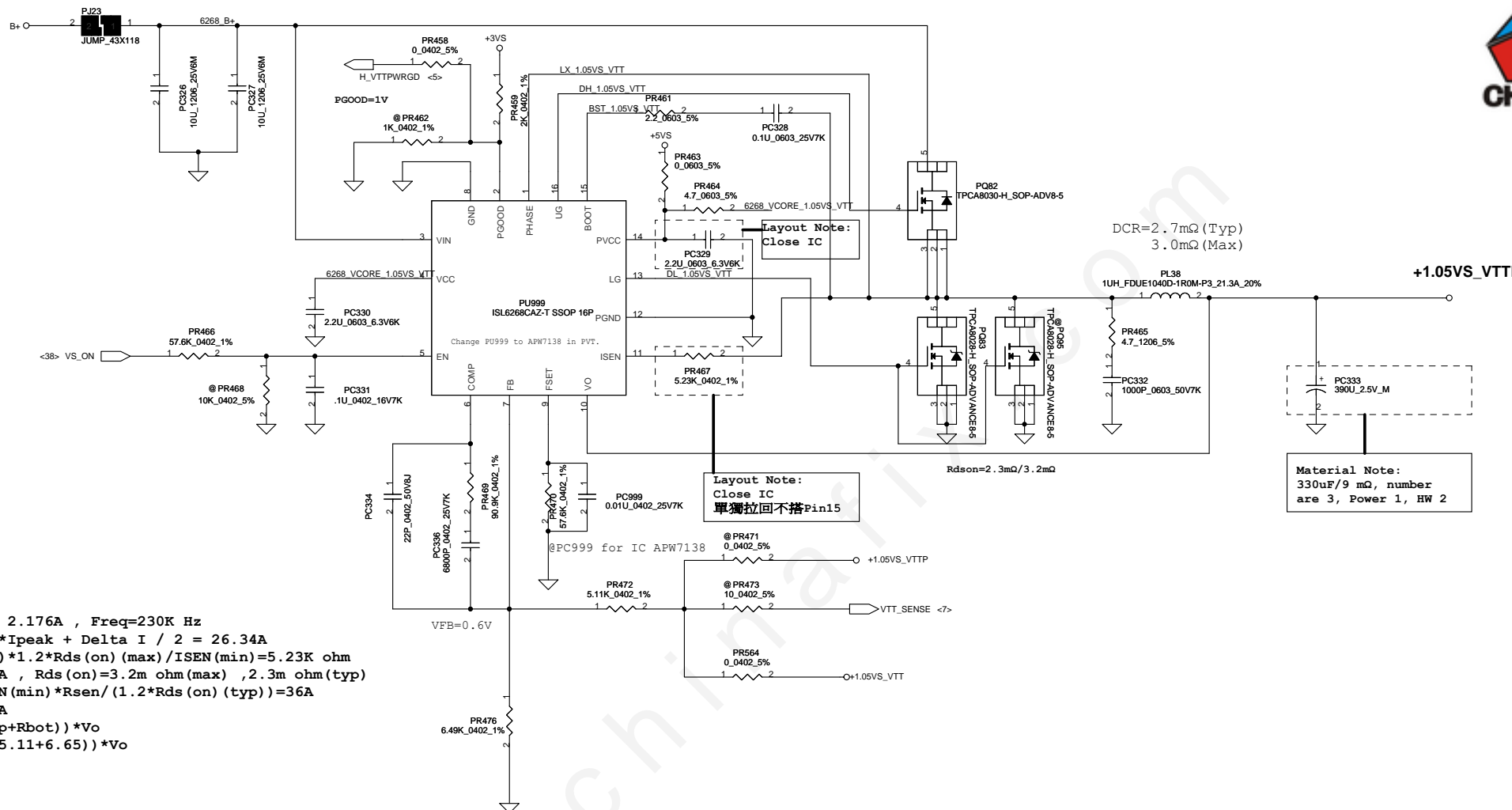
VFB=0.75V
 $V_o = VFB * (1 + PR418 / PR419) = 1.52V$
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm
Ipeak=13.61A Imax=9.527A
 $V_{trip} = R_{trip} * I_{0uA} = 0.11V$
 $I_{ocp-min} = V_{trip} / (R_{ds(on)}(max) * 1.2) + \Delta I / 2 = 18.67A$
 $I_{ocp-max} = V_{trip} / (R_{ds(on)}(typ) * 1.2) + \Delta I / 2 = 22.67A$
 $I_{ocpmin} = 18.67A$
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * Freq) = 4.605A$
 $1 / 2 \Delta I = 2.3A$

$I_{ocp} = 18.67A \sim 22.67A$

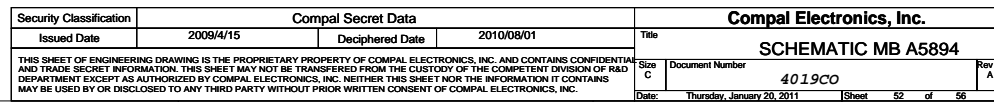
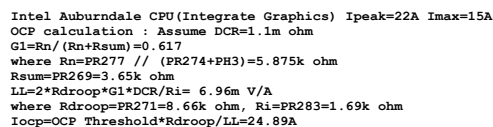
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				Date	Thursday, January 20, 2011
				Sheet	49 of 56

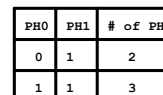




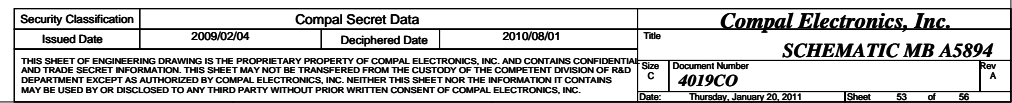
```
+1.05VS_VTT
Ipeak=20.14A
Imax=14.10A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=1.2*Ipeak + Delta I / 2 = 26.34A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=5.23K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) , 2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=36A
Iocp=26.34~36A
Vref=(Rb/(Rtop+Rbot))*Vo
=>0.6=(6.65/(5.11+6.65))*Vo
Vo=1.061V
```

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				Document Number	A
				4019C0	
Date:	Thursday, January 20, 2011	Sheet	51	of	56





	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dy
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify VGA_COREP circuit	update VGA_COREP Vout by NV spec.	0.1	50	change PR136 from SD034604280 to SD034499280. Delete PR137 SD034309280.	2010-0615	PVT
2	Modify VGA_COREP circuit	Modify N12PGS to let Vboot=0.975V, that is VID0=0, VID1=1	0.2	50	Change PR138 SD034147280 to SD034118280. Add PR145 SD028100280. delete PR149 SD028100280.	2010-1102	MP
3	Modify +1.5VP circuit	Because run 3Dmark has voltage too low, increase 1.5V.	0.2	49	Change PR419 from SD034576180 to SD034562180. Only for N12PGS.	2010-1102	MP
4							
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23							

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Date: Thursday, January 20, 2011				Sheet	54 of 56

A -->Modify item



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				4019CO	A
Date: Thursday, January 20, 2011		Sheet 55 of 56			

20091214 Modify For N11P-GV2H	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung :SA000035720	H 45K	H 35K	H 30K	L 20K	L 10K	L 15K
64MX16 Hynix:SA000032490	H 45K	H 35K	H 30K	L 15K	L 10K	L 15K
20100113 Modify For N11P-GE1	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung:SA000035720	H 45K	H 35K	H 10K	L 20K	L 10K	L 15K
64MX16 Hynix:SA000032490	H 45K	H 35K	H 10K	L 15K	L 10K	L 15K
20100601 Modify For N11P-GE	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung:SA000035720	H 45K	L 35K	L 10K	L 20K	L 10K	H 15K
64MX16 Hynix:SA000032490	H 45K	L 35K	L 10K	L 15K	L 10K	H 15K
128MX16 Samsung:SA00003MQ40	H 45K	L 35K	L 10K	L 45K	L 10K	H 15K
128MX16 Hynix:SA00003VS10	H 45K	L 35K	L 10K	L 35K	L 10K	H 15K
20100909 Modify For N12P-GS VRAM: DDR3 900 down to 800	strap0	strap1	strap2	strap3	strap4	ROM_SI ROM_SO ROM_SCLK
64MX16 (800) Samsung:SA000035720	H 45K	H 35K	L 25K	NC	NC	L 10K L 10K H 15K
64MX16 (800) Hynix:SA000032490	H 45K	L 35K	L 25K	NC	NC	L 5K L 10K H 15K
64MX16 (800) Samsung:K4W1G1646G-BC11 SA00004GS10	H 45K	L 35K	L 25K	NC	NC	L 20K L 10K H 15K
64MX16 (800) Hynix:H5TQ1G63DFR-11C SA000041S40	H 45K	L 35K	L 25K	NC	NC	L 15K L 10K H 15K
128MX16 (800) Samsung:SA00003MQ40	H 45K	H 35K	L 25K	NC	NC	L 45K L 10K H 15K
128MX16 (800) Hynix:SA00003VS10	H 45K	H 35K	L 25K	NC	NC	L 35K L 10K H 15K
128MX16 (800) Samsung:K4W2G1646C-HC11 SA000047Q20	H 45K	L 35K	L 25K	NC	NC	L 45K L 10K H 15K
128MX16 (800) Hynix:H5TQ2G63BFR-11C SA00003YO20	H 45K	L 35K	L 25K	NC	NC	L 35K L 10K H 15K
20101220 Modify For N12P-GV VRAM: DDR3 900 down to 800	strap0	strap1	strap2	strap3	strap4	ROM_SI ROM_SO ROM_SCLK
64MX16 (800) Samsung:K4W1G1646G-BC11 SA00004GS10	H 45K	L 35K	L 5K	L 5K	L 10K	L 20K H 10K H 5K
64MX16 (800) Hynix:H5TQ1G63DFR-11C SA000041S40	H 45K	L 35K	L 5K	L 5K	L 10K	L 15K H 10K H 5K
128MX16 (800) Samsung:K4W2G1646C-HC11 SA000047Q20	H 45K	L 35K	L 5K	L 5K	L 10K	L 45K H 10K H 5K
128MX16 (800) Hynix:H5TQ2G63BFR-11C SA00003YO20	H 45K	L 35K	L 5K	L 5K	L 10K	L 35K H 10K H 5K

ROM_SI , 爲Vram配打電阻

BOM Config

PEW71 SKU N11P-GE 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GE@,NonOPT@	431869BOL21
PEW71 SKU N11P-GV2H-A3 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GV2H@,GV2HA3@,NonOPT@,NonGE@	431869BOL22
PEW51 SKU N11P-GV2H-A3 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GV2H@,GV2HA3@,NonOPT@,NonGE@	431869BOL31
PEW51 SKU N11P-GE 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GE@,NonOPT@	431869BOL32
PEW51 SKU N11P-GE 2G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GE@,NonOPT@	431869BOL33
PEW71 SKU N11P-GE 1G Optimus without 3G	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,X7621@,GE@	431869BOL23
PEW71 SKU N11P-GE 2G Optimus without 3G	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,X7601@,GE@	431869BOL24
PEW71/91 SKU N12P-GS 1G Optimus without 3G	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,X7621@,GS@	431869BOL26
PEW71/91 SKU N12P-GS 2G Optimus without 3G	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,X7601@,GS@	431869BOL27
PEW51 SKU N12P-GS 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GS@,NonOPT@	431869BOL34

以上爲LA5893PR10 , Footprint:GB1-128

SMT MB A5894 PEW71 GS OPT 1G WHDMI	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,GS@	4319COBOL01
SMT MB A5894 PEW71 GS OPT 2G WHDMI	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,GS@	4319COBOL02
SMT MB A5894 PEW71 GV OPT 512M WHDMI	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,GV@	4319COBOL03
SMT MB A5894 PEW71 GV OPT 1G WHDMI	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,GV@	4319COBOL04

以上爲LA5894PR10 , Footprint:GB2-128 Compability GB2B-128

PCB ZZZ	GV2HA2@ U51	GV2HA3@ U51	GE1@ U51
LA-5894P REV0 MB	N11P-GV2H-A2_BGA969	N11P-GV2H-A3_BGA969	N11P-GE1-A3 BGA 969P

GE@ U51	GS@ U51	GV@ U51
N11P-GE-A1 BGA 969P	N12P-GS-A1 BGA 973P	N12P-GV-OP-B-A1 BGA 973P

ZZZ3 X7601@ X76248BOL01	ZZZ2 X7622@ X76198BOL22
ALT. GROUP PARTS 2G HYN	ALT. GROUP PARTS 1G HYN

ZZZ1 X7621@ X76198BOL21
ALT. GROUP PARTS 1G SAM

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Date: Thursday, January 20, 2011				Sheet	56	of 56